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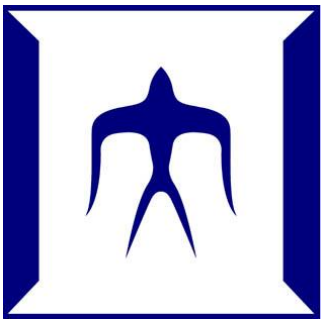

A Study of High-Speed Direct Digital Frequency Synthesizer Solutions in CMOS Technology

by

Abdel Martinez Alonso

A Ph.D. dissertation submitted in partial satisfaction of the requirements for the degree of

Doctor of Philosophy

in

Physical Electronics

in the

Graduate School of Science and Engineering

of

Tokyo Institute of Technology

Supervised by

Prof. Akira Matsuzawa and Prof. Kenichi Okada

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In memory of my beloved father who shared his faith in future with me.

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ABSTRACT

This dissertation describes the trends and limitations of the direct digital frequency synthesizer (DDFS) technology and the design methodology aimed to maximize the throughput in CMOS-based DDFSs. High-speed architectures for a phase accumulator, a phase to amplitude converter, and a two-times interleaved resistive digital to analog converter featuring a random swapping thermometer coding dynamic element matching core are discussed. Solutions for high-speed digital modulations are also integrated. Three proof-of-concept chips confirm the merits of the proposed approach. To begin, a 2GS/s synthesizer consuming only 59mW/(GS/s) is reported. The first CMOS-based DDFS achieving a 7GS/s operation is also characterized. Finally, the only DDFS solution supporting 7GS/s and featuring frequency, phase and amplitude modulations is demonstrated. The potential applications of these developments are also discussed.

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CHAPTER 1:

TRENDS AND LIMITATIONS OF THE DIRECT DIGITAL FREQUENCY SYNTHESIS TECHNOLOGY

The concept of direct digital frequency synthesis was first introduced by J. Tierney in 1971 [1]. It can be defined as a digital signal processing (DSP) technique intended for representing a digital pattern in the analog domain based on a fixed clock period (frequency). The standard direct digital frequency synthesizer (DDFS) is a mixed signal device that generates a sinusoidal waveform at its output [1]. The phase step information contained in the frequency control word (*FCW*) is integrated by a phase accumulator (PA) and transformed into sinusoidal amplitude samples by a phase to amplitude converter (PAC). The digital unit conformed by concatenating the PA and the PAC blocks is also commonly identified in the literature as a numerically controlled oscillator (NCO). The digital representation of the sinusoidal waveform is transformed to the analog domain by using a linear digital to analog converter (DAC). This conventional architecture is often called digital-mapping DDFS (DM-DDFS) and its block diagram is represented in Fig. 1.1. The integration of a DAC and an NCO core in a single chip is frequently known as a complete-DDFS-solution.

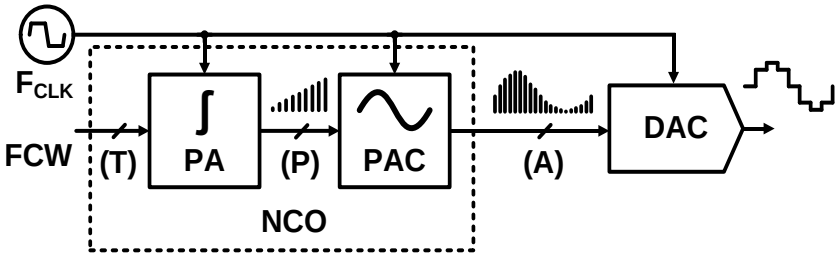


Fig. 1.1. Conventional DM-DDFS architecture.

Where:

- *T*: Tuning word length.
- *P*: Phase word length.
- *A*: Amplitude word length.

Among others, four fundamental equations can be used to characterize the DDFS performance. The relationship between the *FCW*, the system clock frequency, and the tuning word length forms the basic tuning equation for conventional DDFS [2]:

$$F_{OUT} = \frac{FCW \cdot F_{CLK}}{2^{\mathrm{T}}} \tag{1.1}$$

Where:

- F_{OUT}: DDFS output frequency.
- F_{CLK}: System clock frequency.

A baseline study given in [3] has demonstrated how the magnitude of the phase truncation spurs has an upper bound that is determined by the number of bits in the phase word.

$$SFDR \approx 6.02P\ dBc \tag{1.2}$$

Additionally, the amplitude of the DDFS output will be also distorted as a result of the periodical overflow in the phase accumulator circuit. This behavior will create a "rolling" amplitude value at the output of the PAC block. The effect on the analog output is similar to the one observed in an amplitude modulated carrier. The frequency of the modulating signal can be determined as [4]:

$$F_{envelope} = \frac{2^{T-1} mod\ FCW}{2^{T-1}} \cdot SR \tag{1.3}$$

Where:

- $F_{envelope}$: frequency of the modulating signal.
- *SR*: sampling rate.

The numerical analysis disclosed in [5] leads to a theoretical limit of the signal to noise ratio (SNR) determined by the amplitude word length as (DC to *SR*/2):

$$SNR = 6.02A + 1.76\ dB \tag{1.4}$$

The overall system performance depends on both the DDFS and the DAC characteristics. The maximum operating frequency, area, and power consumption are typically limited by the digital components of the DDFS. On the other hand, dynamic performance is mainly determined by the DAC, providing that low phase truncation

spurious-free dynamic range (SFDR) and proper timing are guaranteed in the DDFS core.

1.1 Overview of high-speed DDFS architectures

Multiple high-speed DDFS architectures have been published since the idea was first introduced by Tierney et al. in 1971 [1]. These topologies can be categorized into three groups according to the way the phase to amplitude conversion is implemented (Fig. 1.2). In all cases, the first block is a phase accumulator unit that integrates the *FCW* value to generate a phase ramp digital signal. In the analog mapping architecture (AM-DDFS), the phase to amplitude conversion is performed by using a linear DAC and an analog mapper circuit. The dependency on process, voltage, and temperature (PVT) variations of the analog mapper circuit limits the accuracy of this method [6]. The second approach employs a sine-weighted non-linear DAC (NLD-DDFS). The complexity of the sine-weighted DAC is higher than a linear one and its design becomes challenging when requiring higher amplitude resolution (≥ 12 bits) [6]. Operation speeds up to 32GS/s have been reported in radar applications implementing these two methods in compound semiconductor technologies [7]. It should be noticed that when using the previously described architectures the phase to amplitude conversion is implemented in the analog domain. Consequently, amplitude modulation (AM) can't be performed in the digital domain [8].

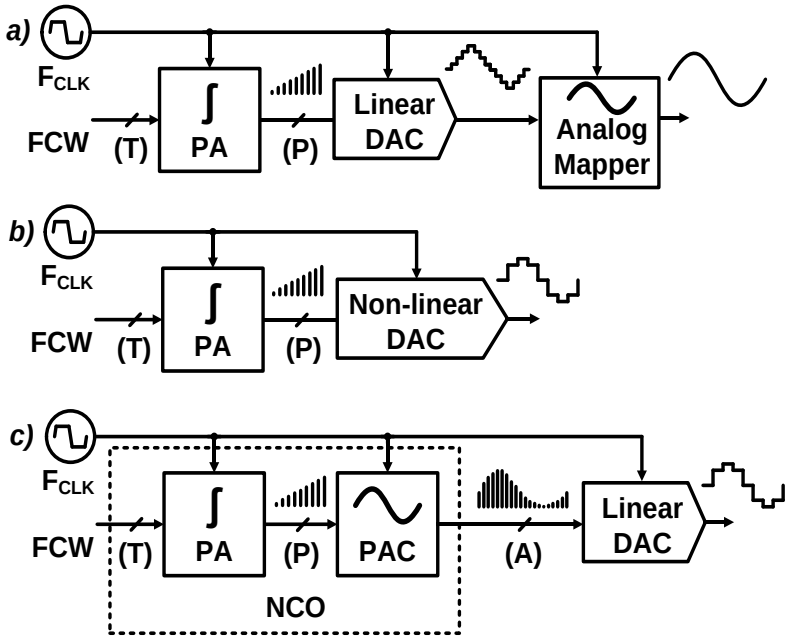


Fig. 1.2. High-speed DDFS architectures. a) AM-DDFS. b) NLD-DDFS. c) DM-DDFS.

The DM-DDFS demands to pre-store the sinusoid digital values in a PAC block and typically exhibits a slow operation speed. The highest sampling rate reported in CMOS technology is only 2GS/s [9]. However, this is a robust digital intensive method that can benefit from the increasing integration density along with the transistor gate length scaling. Also, frequency, phase, and amplitude modulations can be implemented in the digital domain [8]. Table 1-1 summarizes some of the features of these architectures and relates them with the characteristics of the most suitable technologies in every case. The AM-DDFS and NLD-DDFS architectures feature a low/medium logic density and can take advantage of the higher carrier mobility in the compound semiconductor materials to boost the performance of the analog sections. The main drawbacks when employing these technologies are an increased power consumption and cost when compared with CMOS technology. On the other hand, the CMOS technology can be combined with the digitally intensive DM-DDFS architecture in order to reduce the power consumption and costs in mass productions.

TABLE 1-1: DDFS ARCHITECTURES AND TECHNOLOGIES.

<table>
<tr><th>Architecture</th><th>Features</th><th>Preferred technology</th></tr>
<tr><td rowspan="2">AM-DDFS</td><td>Low logic density</td><td rowspan="3">SiGe, InP:
+ f_T/f_{MAX} = 406GHz/423GHz in InP [8]
+ Better 1/f noise [10]
- Higher power consumption
- Low integration density
- Higher cost</td></tr>
<tr><td>Analog centric</td></tr>
<tr><td rowspan="2">NLD-DDFS</td><td>Medium logic density</td></tr>
<tr><td>Analog centric</td></tr>
<tr><td rowspan="2">DM-DDFS</td><td>Digital centric
High logic density</td><td rowspan="2">CMOS:
- $f_T/f_{MAX} \approx$ 160GHz/200GHz in 65nm CMOS [11]
- Larger 1/f noise [10]
+ Lower power consumption
+ Higher integration density
+ Low cost in mass production</td></tr>
<tr><td>Reduced analog sections</td></tr>
</table>

Lower f_T/f_{max} and larger *1/f* noise are among the fundamental limitations when compared with SiGe or InP technologies. For that reason, analog sections with reduced complexity and digital compensation techniques should be adopted [10].

1.2 Non-idealities in DM-DDFS solutions

The general model employed to describe the non-idealities in a DM-DDFS can be represented as in Fig. 1.3 [2]. Except in the case of ε_f, these deviations from the ideal model in Fig. 1.2 c) will translate into phase noise and spur contents in the frequency domain. The quantization error inherent to the discrete approximation of the sampling step by a digital *FCW* will result in a fixed offset in the carrier frequency. Previous works have described in detail the effects of these distortions in the synthesized signal [12]-[15]. However, this background is relevant to the analysis of the simulation and measurement results and it will be briefly introduced in the following subsections.

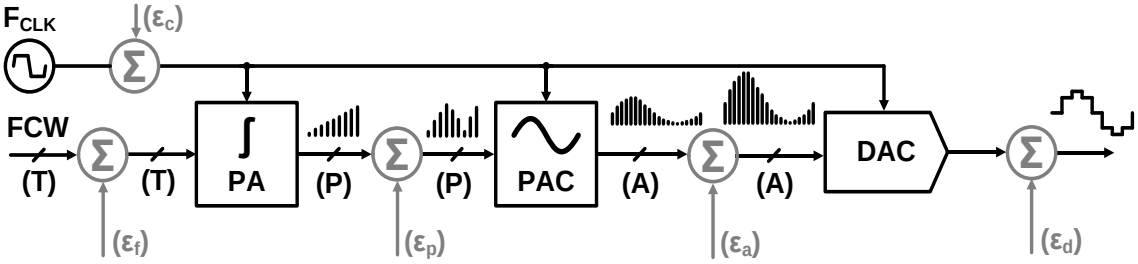


Fig. 1.3. Model of a non-ideal DM-DDFS.

Where:

- $\mathcal{E}_c$: Clock noise.
- $\mathcal{E}_f$: Frequency deviation.
- $\mathcal{E}_p$: Phase-truncation error.
- $\mathcal{E}_a$: Amplitude quantization error.
- $\mathcal{E}_d$: Digital to analog conversion error.

1.2.1 Clock noise

Low phase noise can be achieved because the DDFS acts as a frequency divider

increasing the integration period of the edge jitter [12]. The relationship between the absolute phase noise at the input and output ports follows (1.5) [13]. This theoretical approximation has been confirmed by measurement of different DDFS devices in [12].

$$PN_{improvement} = 20\log_{10}\left(\frac{SR}{F_{OUT}}\right)[\text{dB}] \tag{1.5}$$

The close-in phase noise is limited by the clock source characteristics [12]. Any noise or spurs in the reference signal will be typically reflected in the phase noise characteristics at the DDFS output. The described behavior is represented in Fig. 1.4. It has been generally accepted as a rough model for the phase noise evaluation in DDFS systems [14]. The noise floor of the DDFS circuit will mask the clock contribution at some point and confine this improvement [14]. The expected noise floor of three DDFS having different amplitude word lengths was modeled across different clock frequencies and is represented in Fig. 1.5. It should be noticed that a quantization noise density of about -160dBc/Hz is expected when A = 10 and the system runs at 7GS/s. The quantization noise floor of the DDFS (N_q) was approximated in [2] as:

$$N_q = -(SNR + 10\log_{10}(SR)) \text{ [dBc/Hz]} \tag{1.6}$$

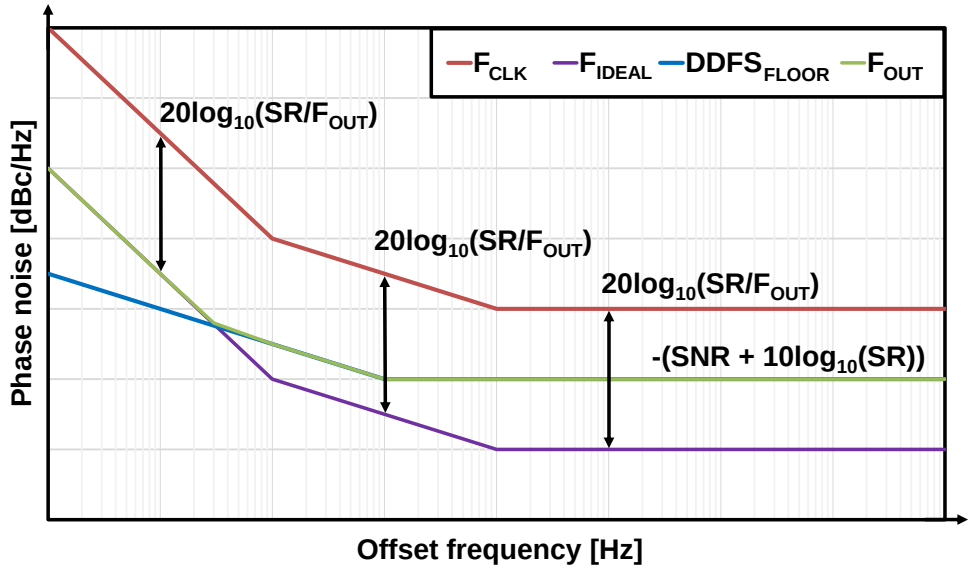


Fig. 1.4. DDFS phase noise model.

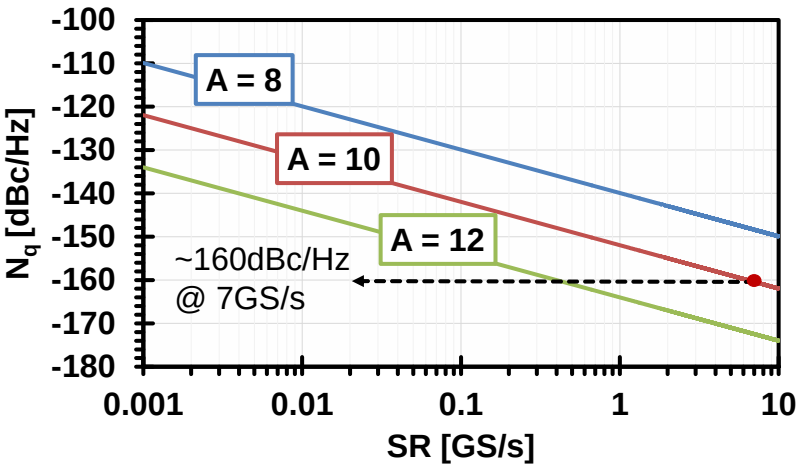


Fig. 1.5. DDFS quantization noise floor.

1.2.2 Phase-truncation errors

As previously mentioned, the phase truncation errors will create a periodic distortion in the output of the PA block that generates spurious contents in the synthesizer output [15]. The maximum theoretical value can be determined by employing (1.2). It should be noticed that this errors can be reduced by increasing the number of bits addressing the PAC block. However, this will also increase the complexity of the phase to amplitude converter circuit. Conventionally, this spur lines are masked by the noise floor of the integrated DAC and do not define the overall wideband SFDR (W-SFDR) performance. As an example, when using a 14x10-bits PAC block, the SFDR degradation due to the truncation errors will have a theoretical maximum value of 84.28dBc (1.2). On the other hand, a high-speed 10-bits DAC will typically exhibit an SFDR performance poorer than the worst case spur due to the phase truncation effect.

1.2.3 Amplitude quantization errors

A periodic and additive distortion will result from the finite resolution that is employed to represent the sine waveform information in the digital domain. Similar to the phase truncation case, this errors can be mitigated by increasing the amplitude resolution of the employed PAC and DAC. However, this will inevitably lead to a growth in the area and power consumption. The magnitude of the generated spurs will depend on the numerical period of the output sequence [15]. In case the repetition ratio of the quantization error is relatively long when compared with the output signal period, the spur will be finely spaced approaching a white noise distribution [15]. A different scenario occurs when the quantization errors are more correlated with the output signal

due to the reduction of the sine waveform period. In that case, it could be possible to have no amplitude quantization errors at all (the processed samples exactly matches the stored values with no quantization errors) or spurious lines having an estimated carrier to spur ratio (C/S) according to (1.7) [15] (assuming maximum quantization error in every sample and all the energy concentrated in one spur):

$$\frac{C}{S} = -3.01 + 6.02A \text{ [dBc]} \tag{1.7}$$

Where:

- A: Number of bits at the PAC output.

According to this analysis, the expected worst case spur due to the correlated amplitude quantization errors should be below 57.19dBc when employing a 10-bits DAC.

1.2.4 Digital to analog conversion errors

The static and dynamic performance of the integrated DAC will ultimately define the spectral purity of the generated carrier. The mismatch between the elements employed as references for the digital to amplitude conversion can generate non-linear distortions that will affect the SFDR characteristics. However, in high-speed applications, the determinant factor is typically the dynamic performance. The artifacts resulting from incomplete settling times, code-dependent switching activity, induced power supply noise, clock feedthrough, imperfect switching time, output or input impedance modulation effects and other anomalies are typically stronger than those having a static nature.

1.3 State of the art

In Fig. 1.6 a selection of the best performance complete-DDFS-solutions reported since 2004 up to date is represented. Three main areas can be highlighted among the most widespread applications: regions (I), (II) and (III). The first one is defined by low-speed and low-power devices with a high SFDR. These features are increasingly demanded by portable and handled applications such as the baseband processing in Bluetooth transceivers [16]. Medium to high resolution (10 to 16 bits) digital-mapping direct DM-DDFSs are frequently employed in this group (the phase to amplitude conversion is performed in the digital domain).

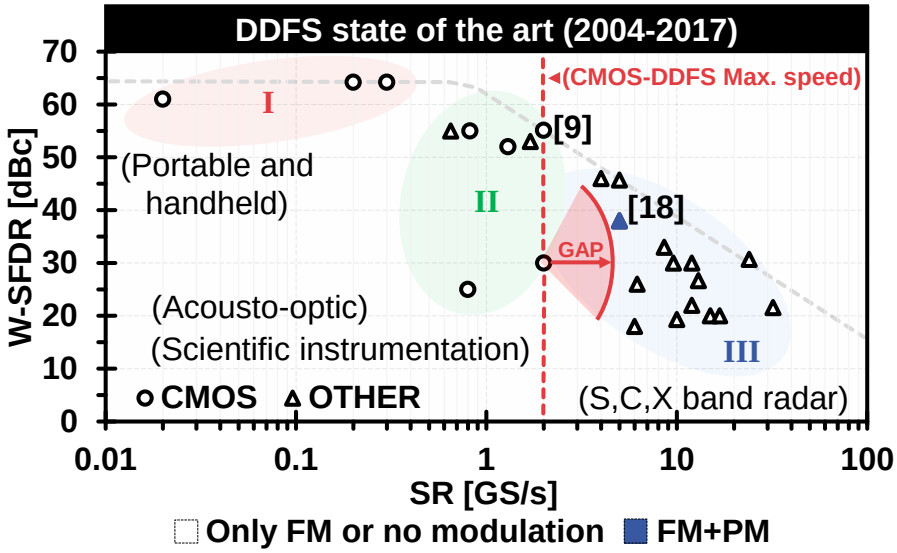


Fig. 1.6. Complete-DDFS-solutions performance.

Since the clock frequency is relatively low, the penalty in energy consumption is less restrictive. In region (II), the most commonly used architectures are medium amplitude resolution (9 to 12 bits) DM-DDFS topologies and NLD-DDFSs. Fine frequency tuning resolution and high integration density can be achieved when using these solutions. These advantages are fully exploited in applications like acousto-optic radio frequency (RF) drivers [17] and scientific instrumentation. However, with clock frequencies up to about 2GHz, these synthesizers can barely cover the very high frequency (VHF) and ultra high frequency (UHF) bands.

Continuously motivated by the advance in the compound semiconductor manufacturing process (reaching a f_T/f_{max} of more than 300GHz/300GHz [4], [7]), the high-speed solutions have been exclusively dominated by these technologies. Low-resolution (5 to 8 bits) AM-DDFSs [6] or NLD-DDFS architectures [4], [7], [18] are commonly employed in the region (III). In both cases, the phase to amplitude conversion is implemented in the analog domain. Radar and frequency exploration systems operating in the S, C, and X bands require high output frequency, fine frequency resolution, fast channel switching and versatile frequency and phase modulation capabilities [18]. This performance can be achieved by implementing DDFS architectures in indium phosphide (InP) double heterojunction bipolar transistor (DHBT)) [7], [19] or silicon germanium (SiGe) technologies [4], [6], [18]. However, the applicability of these solutions is limited by the higher fabrication costs and more difficult access to foundry services. Additionally, amplitude modulation can't be performed in the digital domain when using these architectures. Only one design in

region III has reported frequency and phase modulations [18]. As a consequence, these approaches has been scarcely used in other application areas.

Although silicon complementary metal oxide semiconductor (CMOS) has become a mature and cost-effective technology, DDFS applications have been limited to regions I and II. The highest sampling rate (*SR*) among on-silicon CMOS-based DDFSs is only 2GS/s [9]. Due to these performance limitations, CMOS-based DDFS applications have been almost exclusively restricted to the VHF and UHF bands as defined by the Institute of Electrical and Electronics Engineers (IEEE) [20]. As a result, a performance gap can be observed between the state of the art of CMOS-based DDFSs and those devices implemented in compound semiconductor technology (Fig. 1.6).

Several commercial DDFS solutions are currently available [21]-[24]. The maximum supported sampling rate among these devices is 6GS/s [23] (Fig. 1.7). Also, the best-reported power efficiency among these commercially available chips is about 390mW/(GS/s) [23]. The power consumption of the solutions operating in excess of 2GS/s in Fig. 1.8 is above 1W. It can be also noticed from Fig. 1.7 that several solutions integrate frequency, phase and amplitude modulation capabilities. However, the maximum sampling rate among this group is only 3.5GS/s [21]. This fact limits its practical application to systems operating up to about 1.4GHz (40% of the *SR*).

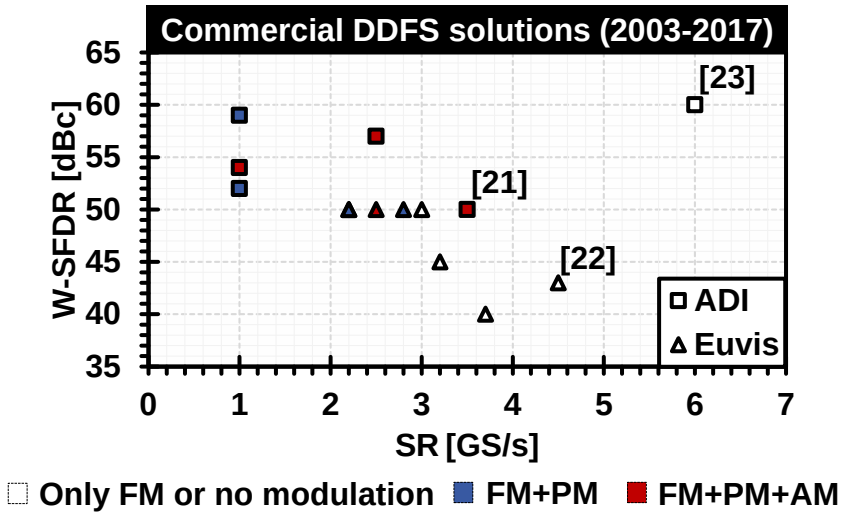


Fig. 1.7. W-SFDR performance of commercially available complete-DDFS-solutions.

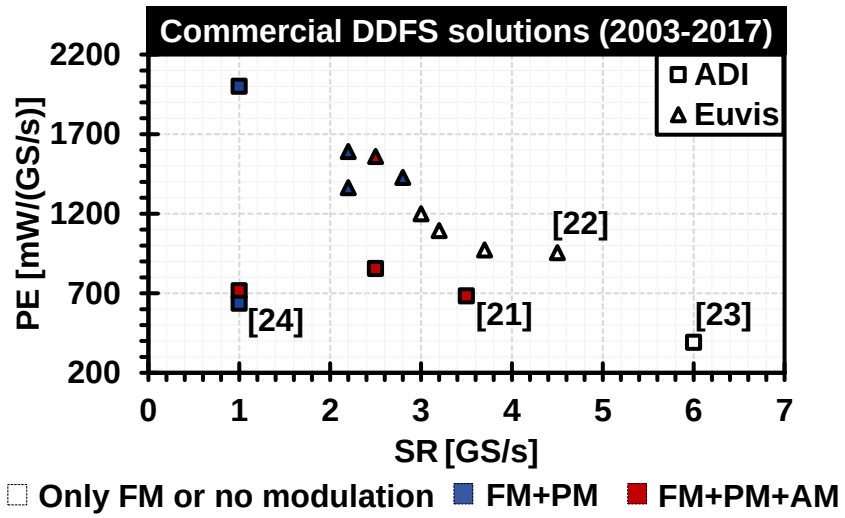


Fig. 1.8. PE performance of commercially available complete-DDFS-solutions.

1.4 DDFS applications in radar technology

The linear frequency modulation (LFM) has been widely employed in frequency modulated continuous wave (FMCW) radars for determination of the actual range to a target [25]. This technique consists of generating a chirp signal and take the frequency difference between the transmitted and received waves after the downconversion [25] (Fig. 1.9). The range resolution (R_{RES}) of the FMCW radar has been defined as [25]:

$$R_{RES} = \frac{c}{2B_{TX}} \tag{1.8}$$

Where:

- *c:* Speed of light.
- B_{TX}: Bandwidth of the transmitted chirp.

The R_{RES} can be reduced by increasing the $B_{TX,}$ which, at the same time, can be extended by spreading the frequency deviation of the generated chirp signal ($f_3 - f_0$ in Fig. 1.9). Since the range information is obtained from this frequency difference between the transmitted and received chirps (Δf), the linearity of the generated frequency modulation is of primary concern [25].

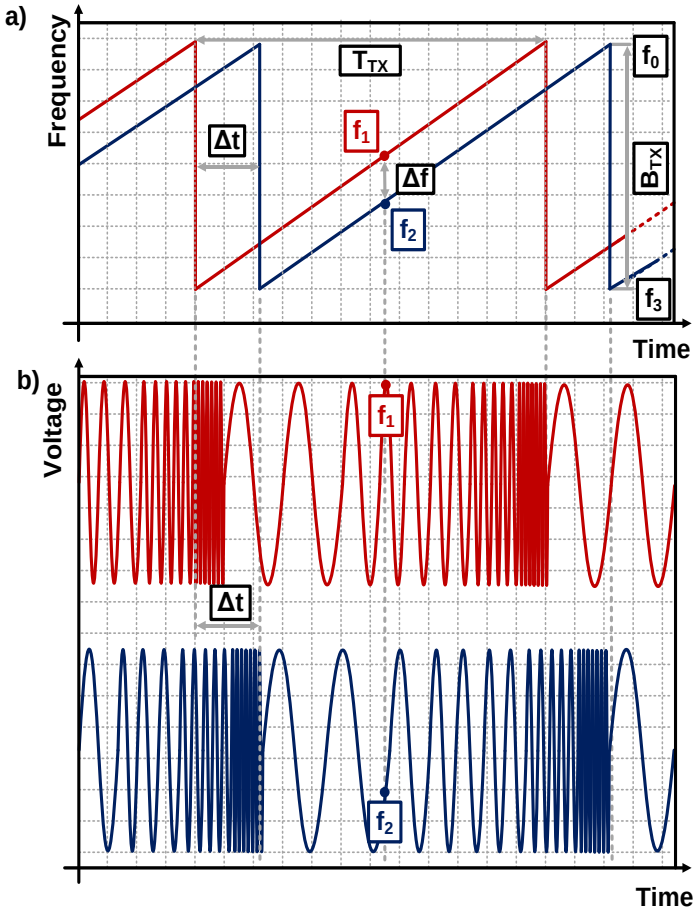


Fig. 1.9. Generated and received chirp signals. a) Frequency domain. b) Time domain.

Where:

- Δf: Frequency difference between the transmitted and received chirps (f_2-f_1).
- Δt: Time difference between the transmitted and received chirps.
- T_{TX}: Chirp length.

Different FMCW radar transmitters have been proposed [25]-[30], all of them having its own advantages and disadvantages. Topologies based on voltage controlled oscillators (VCO) were introduced in [26]-[28] (Fig. 1.10). Difficulties in controlling the gain of the VCO circuit typically limits the linearity of this approach. Process, voltage and temperature variations will also affect the performance of this circuit [25]. The frequency resolution is mainly determined by the VCO tuning sensitivity and the accuracy of the control voltage generator. The settling time is limited by the response time of the VCO (typically in the ns range).

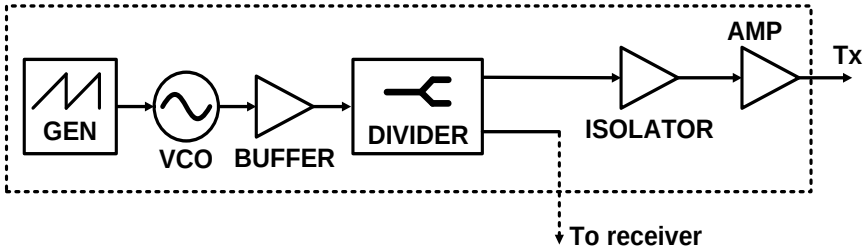


Fig. 1.10. VCO-based FMCW radar transmitter.

A second approach consists on implementing a hybrid DDFS-PLL system in which the DDFS core generates the chirp information for the frequency multiplication in the phase locked loop (PLL) [29], [30] (Fig. 1.11). A more linear frequency sweep and better immunity to PVT variations can be achieved by using this topology (locked to the accurate DDFS output) [30]. However, its inherent loop delay, limited frequency resolution (the DDFS resolution is multiplied by N in the PLL loop), and discontinuous-phase switching will translate in challenges when targeting a fast and wideband linear chirp signal [31]. Additionally, the use of a PLL will negatively impact the phase noise performance [14]. Another possible solution is to make use of a high-speed radio-frequency DAC (RF-DAC) [32] dynamically controlled by an external digital signal processing unit implemented in a field-programmable gate array (FPGA) device (Fig. 1.12).

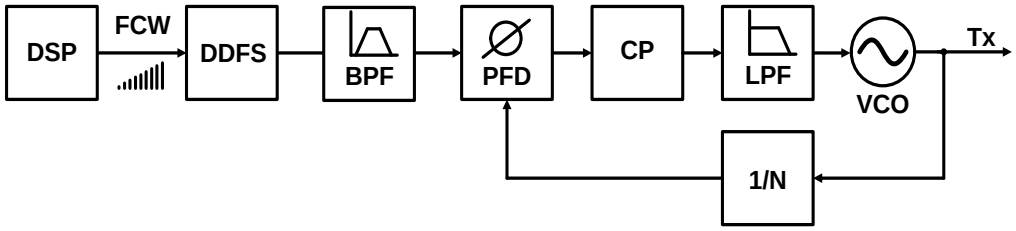


Fig. 1.11. DDFS-PLL hybrid FMCW radar transmitter.

Where:

- *BPF:* Band-pass filter.
- *PFD:* Phase frequency detector.
- *CP:* Charge pump.
- *LPF:* Low-pass filter.
- *1/N:* Feedback divider.

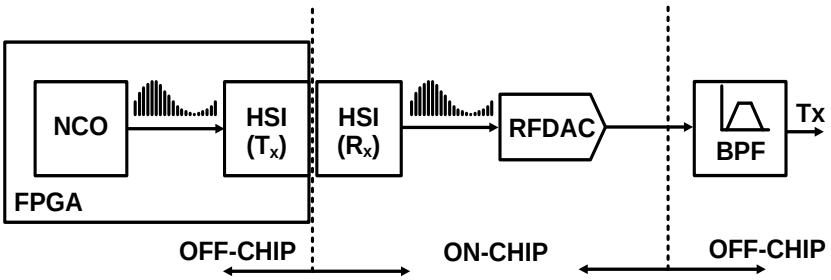


Fig. 1.12. FPGA+RF-DAC based FMCW radar transmitter.

Although this is a feed-forward structure that does not suffer from any delays associated with feedback loops, the power consumption is typically higher compared with other solutions. The dissipated energy is increased as a result of the high-speed interfaces (HSI) required to control the RF-DAC [33]. This system can be also understood as a discrete DDFS solution (with an increased cost in terms of the bill of materials and printed circuit board (PCB) complexity). Also, as demonstrated in [34], digital circuits implemented in FPGAs devices consume approximately 35 times larger area, 14 times more dynamic power and have between 3.4 to 4.6 times slower performance compared with ASIC implementations in equivalent technologies.

All programmable RF-sampling solutions have been recently reported in 16nm FinFET technology [35]. Power savings can be achieved when removing the need for high-speed interfaces by integrating an RF-DAC core with an FPGA fabric in a system on chip (SoC) solution [35]. However, this programmable structure still suffers from a slower operation speed and higher power consumption due to the general purpose logic required by the FPGA fabric [34]. Finally, high-speed complete-DDFS-solutions can be employed in order to accurately generate linear and wideband frequency chirps [23]. Furthermore, the DDFS reference can be driven by a low phase noise dielectric resonator oscillator (DRO) (Fig. 1.13), resulting in a feed-forward, PLL free, architecture [36]. The use of a direct digital frequency synthesizer offers a highly linear solution. However the maximum $B_{TX,}$ and consequently, the minimum R_{RES}, is limited by the sampling rate of the DDFS [31]. The main benefits and drawbacks of the described FMCW transmitter architectures are summarized in Table 1-2. It should be noticed how the combination of a DRO and a complete-DDFS-solution can result in a system with fine frequency resolution, high linearity, fast and continuous-phase switching and excellent phase noise. Also, since this is a digitally intensive architecture, it is less affected by the aging and thermal drift of the components [15]. Achieving a high throughput while keeping a competitive power efficiency and SFDR performance represents the main challenges when integrating this mixed-signal system.

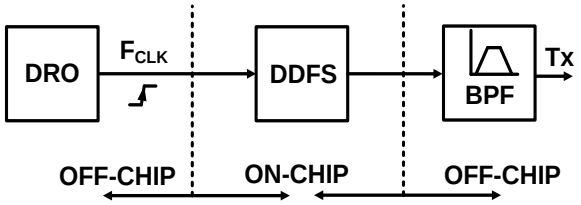


Fig. 1.13. DRO+DDFS based FMCW radar transmitter.

TABLE 1-2: FMCW RADAR ARCHITECTURES.

Architecture	Frequency resolution	Linearity	Switching time	Phase noise	PVT variations/aging	Power consumption	Solution size/footprint
VCO	Medium	Low	Medium	High	High	Low	Small
DDFS PLL	Low	Medium	Slow	Medium	Medium	Low	Medium
FPGA RF-DAC	High	High	Fast	Low	Low	High	Large
DRO DDFS	High	High	Fast	Low	Low	Medium	Medium

1.5 Future evolution of DDFS applications

1.5.1 Radar sensor for unmanned systems.

The use of surface and aerial unmanned systems (US) in civilian applications has an enormous growth potential in the near future. An increasing number of applications have been described [37]. These range from delivery services, industrial robots, and search and rescue missions to unmanned vehicles for agriculture and remote site exploration. It is also expected that the unmanned vehicles traffic will substantially grow in the upcoming years [37]. As a consequence, safety and security issues have been raised when evaluating possible interactions of the USs with conventional manned vehicles. These circumstances will demand the development of new onboard and ground-based sense-and-avoid systems (SAA) as well as traffic monitoring schemes. Among other technologies, such as optical systems, global positioning system (GPS) receivers, and inertial sensors, the radar technology should play an important role in the development of the next generation of collision avoidance systems [38]. One important advantage of the radar-based sensors compared with optical systems is that they are not affected by the ever-changing meteorological conditions. In the same way that radar technology has played an important role in large-scale air traffic control, it has the potential to be employed in miniaturized frequency exploration systems for unmanned vehicles. Although at present time the standards and requirements of this new radar generation for USs are still not available, some experimental results in the S-band

(2.4GHz) [39], X-band (9.6GHz) [40], Ku-band [41] and Ka-band (35GHz) [42] have been reported. Among other technologies such as phase locked loops, the direct digital frequency synthesis technique has demonstrated to be a suitable solution for high-end radar applications. As illustrated in previous sessions, some of the DDFS benefits are unparalleled settling times (ns range) and tuning bandwidths, continuous-phase frequency switching with sub-Hertz resolution, low phase noise, and frequency/phase modulations in the digital domain. These characteristics have been exploited in conventional radar systems operating in the S, C and X bands [25]. However, there are a number of challenges that need to be addressed in order to fulfill the requirements of the new generation of radar sensors for miniaturized SAA applications.

First, these applications demand a reduction in both the power consumption and area of the high-speed DDFS solutions in order to be incorporated in multiple ground stations or onboard the unmanned vehicles/aircrafts. The direct digital frequency synthesis solutions are often power-hungry (several Watts) and occupy a large silicon area. These drawbacks become more critical in high-speed applications that are typically implemented in compound semiconductor technologies [4], [7]. Second, the DDFS system needs to be integrated into an increasingly digital environment. CMOS technology could potentially be employed in order to cover the required frequency bands while benefiting from its high integration density characteristics.

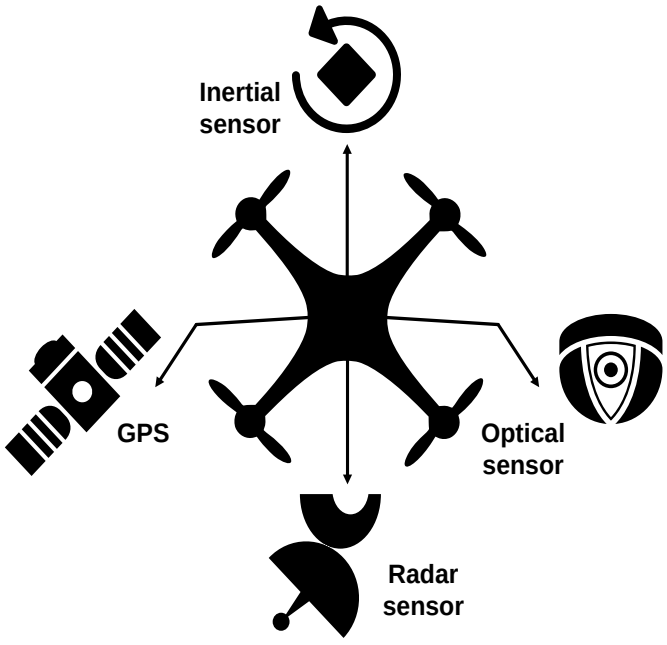


Fig. 1.14. Components of the onboard sense-and-avoid system.

Also, since the DDFS is a sampling system, spurious contents becomes an important issue to be taken into account.

1.5.2 Multi-band multi-standard polar modulator.

In the VHF, UHF and L bands the spectrum resources are very limited. The second generation of digital television (DTV) broadcasting systems is now calling for modulation orders up to 4K-QAM and beyond in order to support the increasing demand for higher data rates imposed by the new high-definition television standards [43]. Similarly, the cable standard DOCSIS 3.1 specifies 4K-QAM and includes 16K-QAM and 64K-QAM for future implementations (Fig. 1.15) [44]. Due to the increase in the modulation order, the minimum required C/N and transmitter modulation error rate (TxMER) are also more demanding [43]. The direct polar modulator (Fig. 1.16) instead of encoding the information into I and Q signals adopts the polar form in which the amplitude and phase of the constellation vectors are digitally generated by a direct digital frequency synthesizer [45]. For this reason, it can be considered I/Q mismatch free architecture. Low phase noise can be also achieved because the DDFS acts as a frequency divider increasing the integration period of the jitter [14]. Finally, all the modulations can be implemented in the digital domain, reducing the need for manual tuning or calibration due to the analog component aging or temperature drift. These are very attractive characteristics that could be potentially used in order to improve the TxMER in SoC transmitters. The direct polar modulator architecture resembles the block diagram depicted in Fig. 1.16.

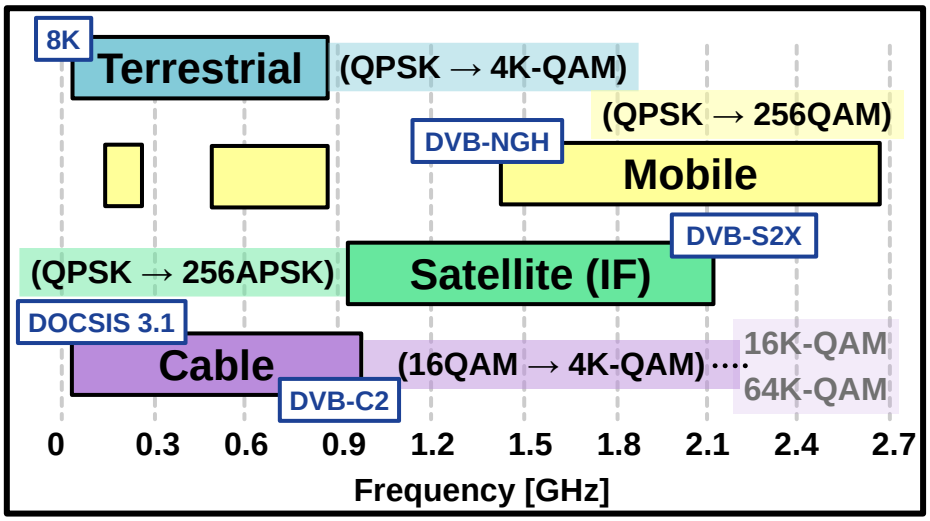


Fig. 1.15. DTV broadcasting systems allocation and evolution.

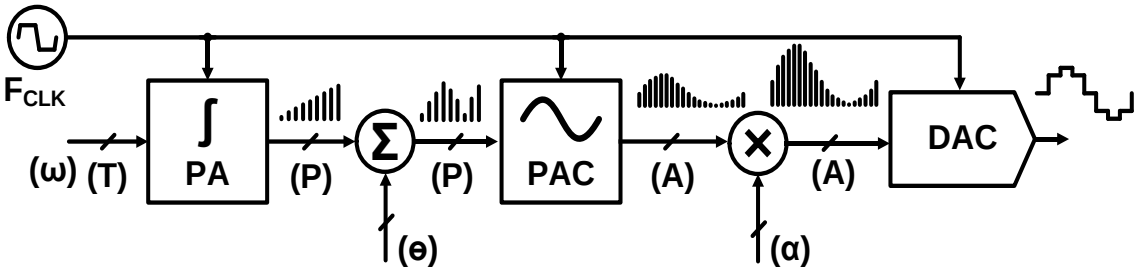


Fig. 1.16. Direct polar modulator architecture.

$$DDFS_{out} = \alpha \sin\left(2\pi\,\omega t + \theta\right) \tag{1.9}$$

It should be noticed that the basic components are the same that can be found in a complete-DDFS-solution (Fig. 1.1). It additionally requires the digital modulation structures to be inserted into the main DDFS channel. These structures are an adder unit and a multiplier circuit employed to implement the digital phase and amplitude modulations respectively. The frequency, phase and amplitude of the output carrier can be digitally adjusted by dynamically changing the variables ω, θ and α in (1.9). However, practical implementations have been restricted by the speed of the digital blocks and the linearity and spurious performance of the DAC. A sampling rate of at least 6.8GS/s is required in order to cover all the broadcasting standards allocated in the VHF, UHF, L and S bands up to 2.7GHz (Fig. 1.17). A synthesizer with those characteristics could be also employed in other applications such as baseband processing in Bluetooth transceivers [16] and acousto-optic drivers [17]. At the same time, a spurious-free dynamic range from 43dBc to 50dBc (depending on the specific application) is required in order to guarantee a minimum level of interference among all the systems allocated in this crowded frequency bands [46] (Fig. 1.16).

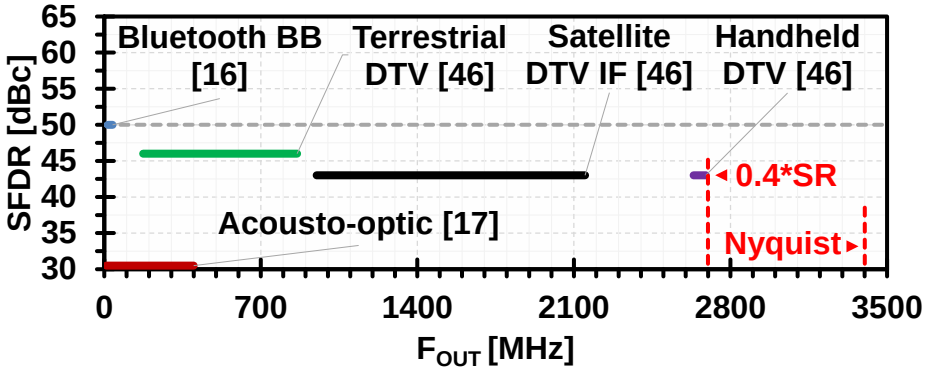


Fig. 1.17. SFDR requirement of systems allocated in the VHF, UHF, L and S bands up to 2.7GHz.

The most important limitation resides in the fact that no DDFS solution with an *SR* ≥ 6.8GS/s and supporting frequency, phase and amplitude modulations has been reported up to date (Fig. 1.6). The only design running at 5GS/s and demonstrating at least frequency and phase modulations was described in [18]. Commercial solutions supporting FM+PM+AM all together has been limited to sampling rates below 3.5GS/s (Fig. 1.7).

1.6 Design challenges of high-speed DDFS solutions in CMOS technology

The main challenges when designing high-speed DDFS solutions in CMOS technology resides in how to increase the system throughput while keeping a competitive power efficiency (PE) and SFDR. The DDFS performance can potentially benefit from the increasing integration density along with CMOS technology scaling by reducing the complexity of the analog sections and employing digital compensation techniques. Shrinking of digital area and reduction of power consumption are still progressing along with the CMOS technology scaling. Furthermore, programmability and accurate predictability of digital technologies give us higher flexibility and robustness [10]. In line with previous statements, DM-DDFS is believed to be the most promising architecture for CMOS-based DDFS implementations. Since the DM-DDFS is a digitally intensive approach, the power consumption typically rises at higher sampling rates. Hence, techniques to reduce the power consumption while increasing the system throughput needs to be developed.

On the opposite side, the difficulty of low voltage operation of further scaled CMOS in analog circuits will be the most serious issue. This results in the saturation of performance and increase of cost [10]. Conventionally, the critical analog component in CMOS-based DM-DDFSs is the DAC. Resistive digital to analog converters are an interesting alternative to the conventional current-steering architectures employed in high-speed DDFSs. Unlike in current-steering based DACs, a rail-to-rail operation can be achieved even under the limited voltage headroom conditions imposed by the continuous CMOS technology scaling. However, mismatches among the resistor units will create non-linear distortions that should be compensated by employing calibration or dynamic element matching techniques.

The sampling nature of the DDFS systems will also generate spurs that fall within the first Nyquist zone. Digital compensation techniques should be implemented in order to improve both the static and dynamic performance of the CMOS-based synthesizers.

The required SFDR for frequency exploration between 9kHz and 300GHz was defined by the International Telecommunication Union (ITU) according to 1.10 [46]. All radar system operating in the previously defined frequency band and with peak envelope power (*PEP*) ≤ 1W requires an SFDR ≥ 43dBc. It should be noticed that, to the best of the knowledge, no specific regulations about unwanted emissions in radar systems for small unmanned systems are currently available. The minimum SFDR requirements for broadcast, satellite and mobile television systems are also defined according to (1.10) in [46] and graphically represented in Fig. 1.17 (assuming PEP ≤ 1W).

$$SFDR = 43 + 10\log PEP, \text{or } 60\,\text{dBc, wichever is less stringent} \tag{1.10}$$

At present time, no device having at least frequency and phase modulation capabilities consumes less than 1W [18], [21]. At the same time, increasing the sampling rate in CMOS based digital designs leads to a proportional surge in the energy consumption. However, the power budget for SAA systems in unmanned vehicles is an increasingly limited resource. Hence, achieving a complete-DDFS-solution with FM+PM+AM capabilities and consuming less than 1W represents a challenge and can pave the way for future integration in onboard sensors.

The target DDFS performance can be summarized as in Table 1-3. A device with these characteristics could be potentially employed both as a radar sensor in SAA systems (up to S-band without using frequency multipliers) and as a multi-band multi-standard polar modulator covering frequencies up to 2.7GHz (40% of the *SR*).

TABLE 1-3: TARGET DDFS PERFORMANCE.

Technology	SR [GS/s]	Modulations			Power consumption [W]	SFDR [dBc]
		FM	PM	AM		
CMOS	≥ 6.8	Yes	Yes	Yes	≤ 1	≥ 43

1.7 Organization of the dissertation

This thesis is focused on the development and evaluation of high-speed solutions for CMOS-based DDFS devices. The manuscript is organized as follows:

In Chapter 1, the trends and limitations of the direct digital frequency synthesizer technology are introduced. Starting with an overview of the high-speed DDFS architectures, the state of the art of this technology is presented. A non-ideal model of a DM-DDFS system is also described. The current status and future evolution of DDFS

applications are also discussed. The main design challenges of high-speed DDFS implemented in CMOS technology are outlined as well. Chapter 2 is focused on the proposed design methodology aimed to maximize the throughput in CMOS-based DDFSs. Descriptions of the most common sequencing methods are included. Emphasis is made on the adopted latch-based digital design. The main techniques introduced in order to achieve the required throughput while keeping a competitive SFDR in the RDAC core are also discussed.

The circuit operation of the digital logic structures is examined in detail in Chapter 3. The description includes a 24-bits complementary dual-phase latch-based phase accumulator and also the proposed dual-phase sum of product terms based phase to amplitude converter. Similarly, in Chapter 4, the 10-bits two-times interleaved RDAC solution introduced in this work is presented. This converter features a high-speed architecture for random swapping thermometer coding dynamic element matching. All the circuit components are analyzed in detail, including the employed hybrid clock distribution network. Chapter 5 is dedicated to the solutions for high-speed digital modulations including a phase-adder and an amplitude-multiplier. Next, in Chapter 6, the proof-of-concept measurement results are analyzed. Three cases of study are presented: a 2GS/s 118mW digital-mapping direct digital frequency synthesizer in 65nm CMOS [47]; a 7GS/s direct digital frequency synthesizer with a two-times interleaved RDAC in 65nm CMOS [48]; and lastly, a high-speed DDFS MMIC with frequency, phase and amplitude modulations also implemented in 65nm CMOS technology [49]. The conclusions and future work are presented in Chapter 7.

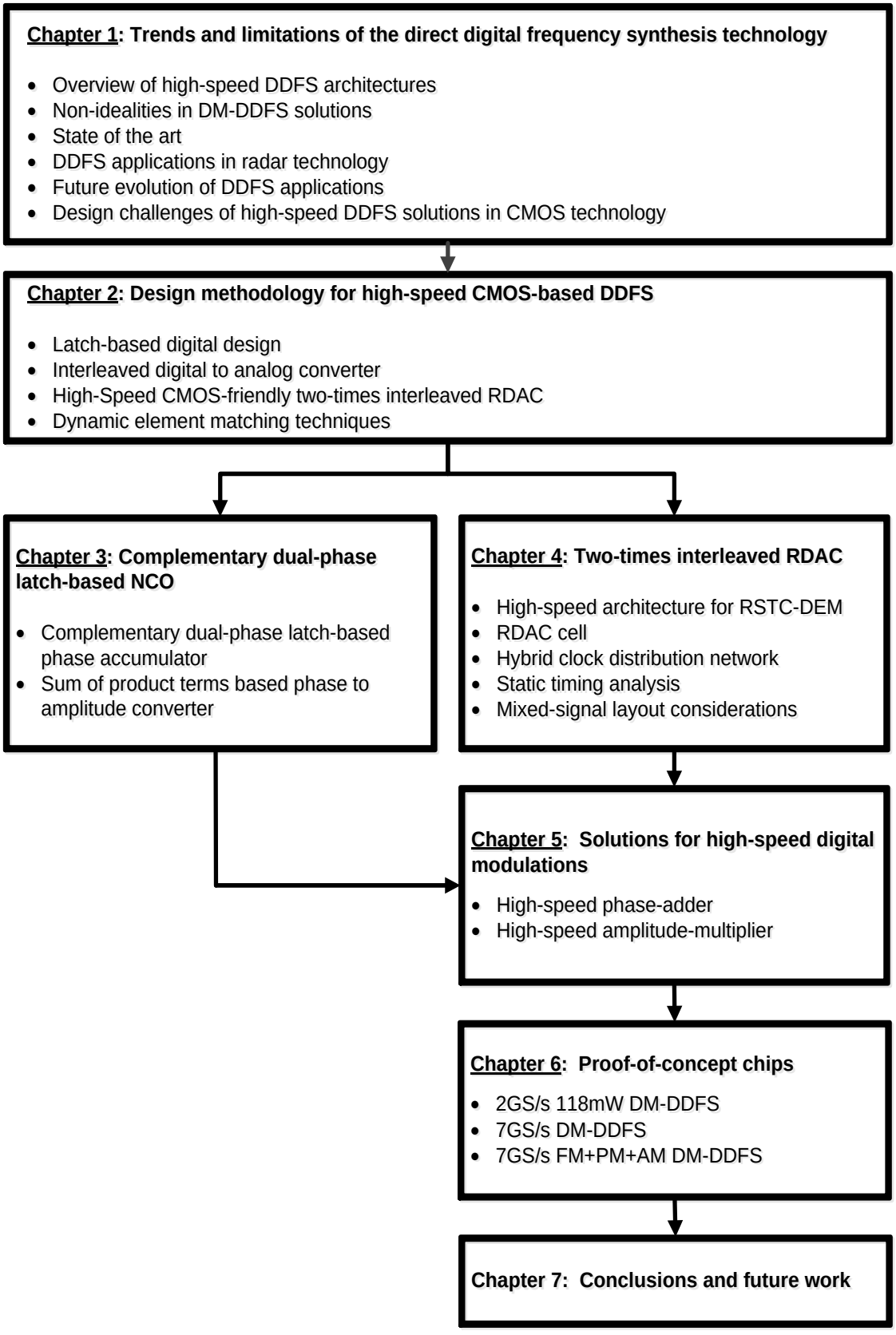
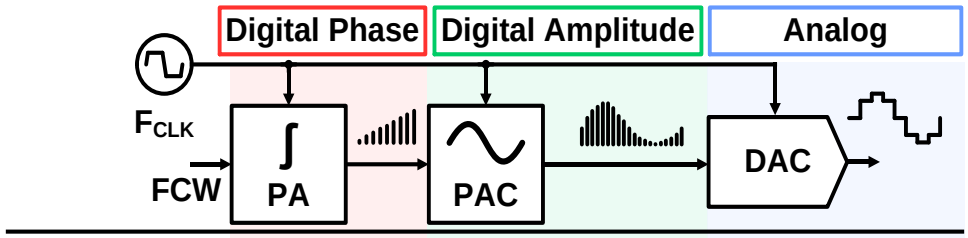


Fig. 1.18. Organization of the dissertation.

CHAPTER 2:

DESIGN METHODOLOGY FOR HIGH-SPEED CMOS-BASED DM-DDFS

Conventionally, DDFS implementations in CMOS technology relies on approximation algorithms [50] or NLD-DDFS architectures [9] in order to increase the throughput. The first approach frequently leads to complex digital circuits that are difficult to speed up by employing parallelism or pipelining techniques. The second approach eliminates the need for a read-only memory (ROM) block (PAC) but increases the complexity of the analog sections (DAC). This imposes additional challenges when employing CMOS technology. Also, flip-flop based architectures have been often selected and almost no other sequencing methods have been explored. As a consequence, up to date, the highest sampling rate among on-silicon CMOS-based DDFSs is only 2GS/s [9]. Although DM-DDFS architectures have been reported in compound semiconductor technologies [19], [51], they are also limited either in power or speed Fig. 2.1. The designs in Fig. 2.1 employs pipelined phase accumulators and current-steering DACs.



[19] InP 24GS/s 19.8W	12b pipelined	ROM-based	Current Steering
[51] SiGe 1.7GS/s 3W	32b pipelined	Linear approximation	Current Steering

Fig. 2.1. DM-DDFS implementations in compound semiconductor technologies.

A ROM-based implementation in InP achieves a 24GS/s record speed for a DM-DDFS [19]. However, the power consumption reaches 19.8W. By using a linear approximation method a SiGe implementation reports 3W [51]. Still, the circuit complexity limits the maximum speed to only 1.7GS/s.

In this work, a different design approach is proposed. First, a complementary dual-phase latch-based DM-DDFS architecture is adopted. This method proves to be advantageous in terms of maximum throughput, power efficiency and yield. Also, the PAC block was generated by employing the sum of product (SoP) terms obtained from a 14×10-bits lookup table. The resulting architecture is a feed-forward digital circuit that can be easily speed up by using intensive pipelining in a complementary and parallel structure. Finally, instead of relying on current-steering data converters, an interleaved RDAC is introduced. Unlike in current-steering based DACs, a rail-to-rail operation can be achieved even under the limited voltage headroom conditions imposed by the continuous technology scaling. This is an important feature in terms of technology portability. The basics of these techniques will be discussed in this chapter. It serves as a preamble for the detailed circuit operation descriptions in Chapter 3.

2.1 Sequencing methods

Several factors need to be taken into account when adopting a sequencing method for high-performance digital designs. Among them, sequencing overhead, skew tolerance, power consumption, area, and simplicity are usually of primary concern. Flip-flops, pulsed latches, and transparent latches have different advantages and disadvantages that will impact the final quality of results [52]. By far, the most popular sequencing method is based on flip-flop devices. Although the timing relationships are quite simple, these systems usually underperform when compared with other approaches. Given its ease of use [52], flip-flops are a good option if, for a certain technology, the throughput or power efficiency requirements are not stringent. However, the ever-increasing demand for higher data rates is constantly reducing the design margins in the available technologies. For that reason, schemes that can push the system performance close to the technology limits are usually required. Transparent latches exhibit lower sequencing overhead and allow almost half a cycle of time borrowing which turns into higher throughputs [52]. Three alternatives are commonly employed: dual-phase nonoverlapping, dual-phase complementary latches and pulsed latches. The difference between the first two methods resides in the way the clock signal is distributed. The former case employs two different clock signals with nonoverlapping

phases to synchronize a pair of consecutive latch elements. In the second case, only one clock signal needs to be distributed and successive latches are enabled during different levels of the clock. Pulsed latches can be viewed as transparent latches with a narrow pulse. They are also capable of a small amount of time borrowing if the pulse is wider than the set-up time. Table 2-1 summarizes the timing characteristics of the previously described sequencing methods [52]:

TABLE 2-1: COMPARISON OF SEQUENCING ELEMENTS.

Sequencing method	Timing overhead ($T_c - T_{pd}$)	Maximum borrowed time (T_b)	Minimum-timing constraint (T_{min})
Dual-phase nonoverlapping	$2T_{pdq}$	$T_{c/2} - (T_s + T_{skew} + T_n)$	$T_h - T_{ccq} + (T_{skew} - T_n)$
Dual-phase complementary	$2T_{pdq}$	$T_{c/2} - (T_s + T_{skew})$	$T_h - T_{ccq} + T_{skew}$
Flip-flop	$T_{pcq} + T_s + T_{skew}$	0	$T_h - T_{ccq} + T_{skew}$
Pulsed latches	T_{pdq}	$T_{pw} - (T_s + T_{skew})$	$T_h - T_{ccq} + (T_{skew} + T_{pw})$

Where:

- T_c: Clock period.
- $T_{c/2}$: Half clock period.
- T_b: Borrowed time.
- T_s: Set-up time.
- T_h: Hold time.
- T_{skew}: Clock skew.
- T_n: Nonoverlapping time.
- T_{pw}: Pulse width.
- T_{pdq}: D-to-Q propagation delay.
- T_{pcq}: Clock-to-Q propagation delay.
- T_{ccq}: Clock-to-Q contamination delay.
- T_{pd}: Logic propagation delay.

A quick analysis of this data reveals that, in terms of timing overhead (extra delay due to the insertion of sequential elements), the pulsed latches and transparent latches are advantageous because they are skew-tolerant (note the absence of the T_{skew} term in the timing overhead equations). Also, latch based designs allow different extents of time borrowing. This situation is different in flip-flop based designs were delays are strictly constrained to less than one clock period ($T_b = 0$). Finally, the dual-phase nonoverlapping method exhibits more relaxed constraints from the minimum timing point of view (T_n will counteract the T_{skew} effects in the clock path). However, the dual-phase complementary method is often used because of the simplicity of the clock distribution [52].

In this work, the dual-phase complementary sequencing method is adopted in order to increase the throughput. Since feed-forward architectures will be implemented in

both the PA and PAC blocks, the timing borrowing property can be extensively used by combining it with pipelining and parallel structures. Another important feature of latch designs is that, in case that not all the available time is consumed by intentional time borrowing, the remaining headroom can be employed to allocate unintended variations due to clock skew and PVT effects. This results in a more robust design compared with flip-flop based architectures [53]. To conclude, Fig. 2.2 shows the comparative data in terms of area and the energy associated with different pins when evaluating equivalent laches and flip-flop cells (65nm CMOS standard-cell library). It should be noticed that up to 43% and roughly 59% and 44% can be respectively saved in terms of the area and the average power consumption of the *D* and *CK* pins when employing 1×-latch cells instead of 1×-flip-flops. The energy associated with the *Q* pin is very similar in both cases. Comparable improvements can be obtained when using other standard cell sizes. These reductions in area and power consumption when employing latches instead of flip-flops in intensively pipelined designs will compensate the extra resources employed in the clock distribution network. As a result, an equivalent power efficiency and a small area penalty can be achieved while reaching nearly twice the sampling rate. The latch-based sequencing methods including the time borrowing mechanisms are explained more in detail in the next section.

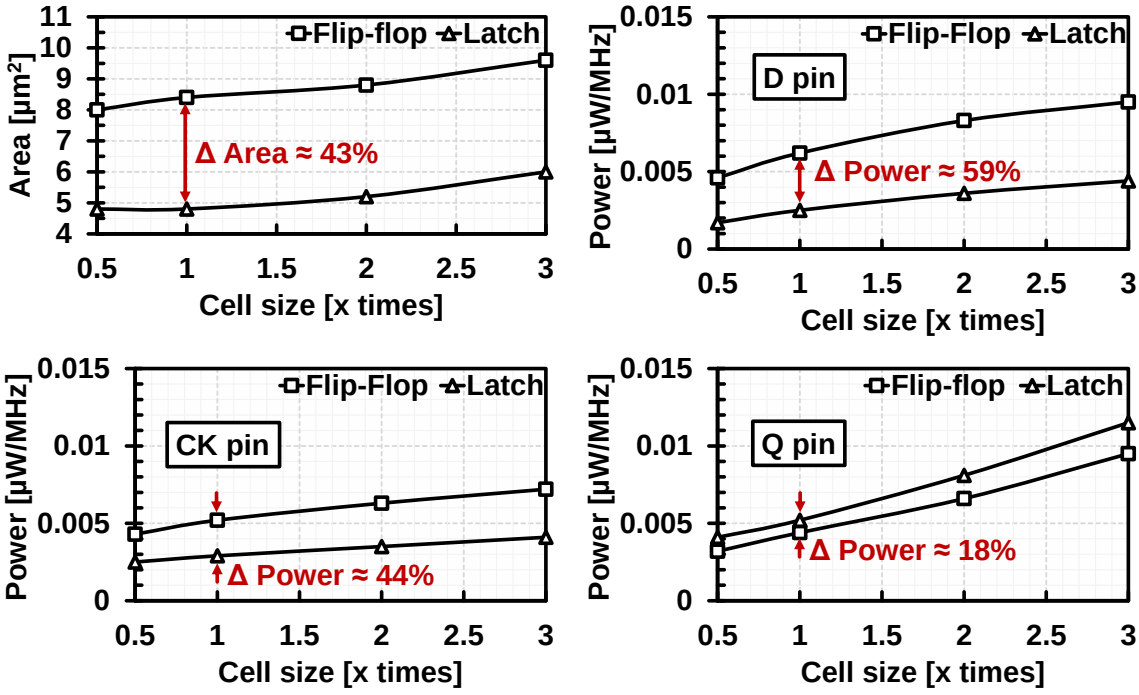


Fig. 2.2. Area and energy associated with different pins of flip-flop and latch cells. Low threshold voltage (LVT), 65nm CMOS standard cell library.

2.2 Latch-based digital design

As previously discussed, the most widely used sequencing methods for latch-based circuits are dual-phase nonoverlapping, dual-phase complementary latches and pulsed latches. The operation scheme of a dual-phase nonoverlapping sequencing method is shown in Fig. 2.3. The first latch is enabled by the clock with P_1 phase. The second latch operates on a complementary and nonoverlapping clock phase (P_2). At no point in time, a transparent period is created between adjacent pipeline stages, eliminating the possibility of races. Data can depart from the first latch on the rising edge of the clock but does not have to set up until the falling edge of the clock on the receiving latch. If one half-cycle has a slower combinational logic, it can borrow time from the next stage. The maximum amount of time that a dual-phase nonoverlapping system can borrow is defined by (2.1) [52]. The complementary dual-phase latch-based design is a special case of the generic dual-phase nonoverlapping sequencing method (Fig. 2.4). Subsequent latches are enabled by different logic levels. The non-overlapping time between the clock phases is zero. The main advantage of this method is the simplicity of the clock generation and distribution. However, if there is a hold time violation, it cannot be fixed by adjusting the non-overlapping time, making prototype debugging more difficult. The maximum amount of time that a complementary dual-phase latch-based system can borrow follows (2.2) [52]. If the maximum borrowed time is kept below this limit, a new data value can be sampled during both high and low levels of the clock.

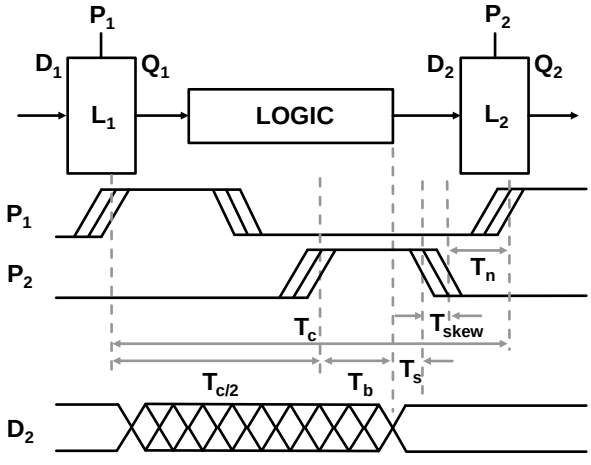


Fig. 2.3. Two-phase transparent latches sequencing method.

$$T_b = T_{c/2} - \left(T_s + T_{skew} + T_n\right) \tag{2.1}$$

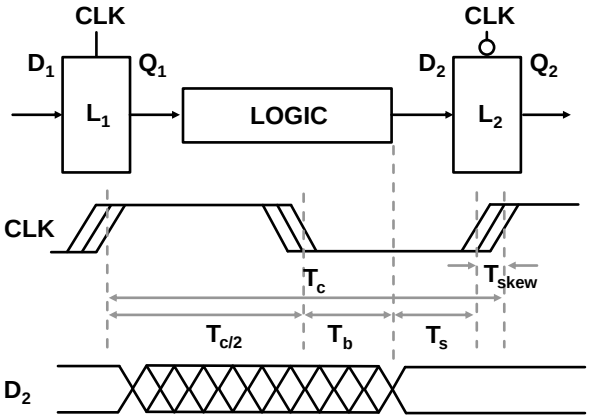


Fig. 2.4. Complementary dual-phase latch-based sequencing method.

$$T_b = T_{c/2} - \left(T_s + T_{skew}\right) \tag{2.2}$$

2.3 Interleaved digital to analog converter

Nyquist-rate DACs achieving up to 11GS/s has been recently reported in CMOS technology [54]. These converters are typically implemented by using a segmented current-steering architecture [54]. The conventional interleaving topology is represented in Fig. 2.5. Two sub-DACs are synchronized with opposite phases of the clock (*CLK*) and share a common output node (*ANALOG_OUT*). The complementary digital inputs are transformed to the analog domain by each sub-DAC. The *DATA_ODD* and *DATA_EVEN* signals control the switches (S_d) that combine the current sources in the *ANALOG_OUT* node according to the digital representation of the waveform. The access to the common output is arbitrated by a second array of switches (S_c) controlled by complementary phases of the reference clock (*CLK*). In this way, the distortion resulting from the code-dependent switching activity can be reduced by disconnecting the output node during the transition time of the S_d switches [54]. The dynamic performance can be further improved by using fully differential structures [54] and dynamic element matching techniques [55]. Since the last interleaving stage is controlled by the *CLK* signal, the skew balance becomes critical in this architecture.

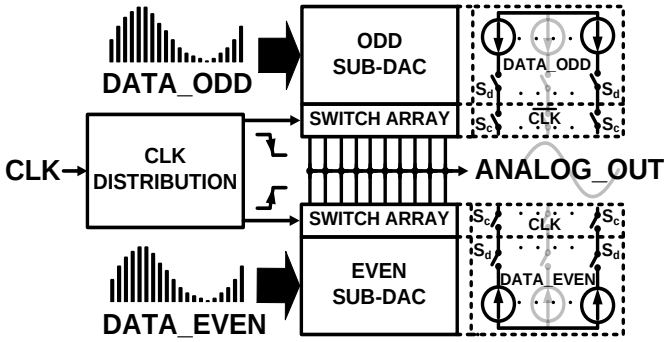


Fig. 2.5. Conventional interleaved DAC architecture.

A study presented in [54] has demonstrated how the errors introduced by the interleaving mechanisms can limit the integrated converter performance. These errors are mainly determined by the matching properties and synchronization between the sub-DACs. Using the same analytical model presented in [54], the W-SFDR degradation introduced by the inter-DAC gain mismatch (ε_{gain}) can be characterized by (2.3). The curves for different gain mismatch profiles are represented in Fig. 2.6. A ε_{gain} around 1% is required in order to achieve an SFDR better than 40dBc in the full Nyquist band when running at 7GS/s. Another source of distortions comes from the duty cycle errors in the reference signal of each sub-DAC in Fig. 2.5 (*CLK*). As demonstrated in [54], a non-50% duty cycle in the reference clock leads to an SFDR degradation following (2.4). As a result, an error smaller than 1ps is needed in order to achieve a W-SFDR better than 40dBc with an output frequency of 2.8GHz sampled at 7GS/s (Fig. 2.7). Similarly, as demonstrated in [56], the SNR performance of the integrated converter will be affected by the sampling errors. The SNR degradation can be modeled according to (2.5). The curves for different output frequencies when having six different RMS jitter profiles in the reference clock are represented in Fig. 2.8.

$$W\text{-}SFDR = 20\log_{10}\left(\frac{1}{\varepsilon_{gain}}\right) + 20\log_{10}\left(\frac{\operatorname{sinc}\left(\frac{F_{OUT}}{SR}\right)}{\operatorname{sinc}\left(\frac{\frac{SR}{2} - F_{OUT}}{SR}\right)}\right) + 6dB \qquad (2.3)$$

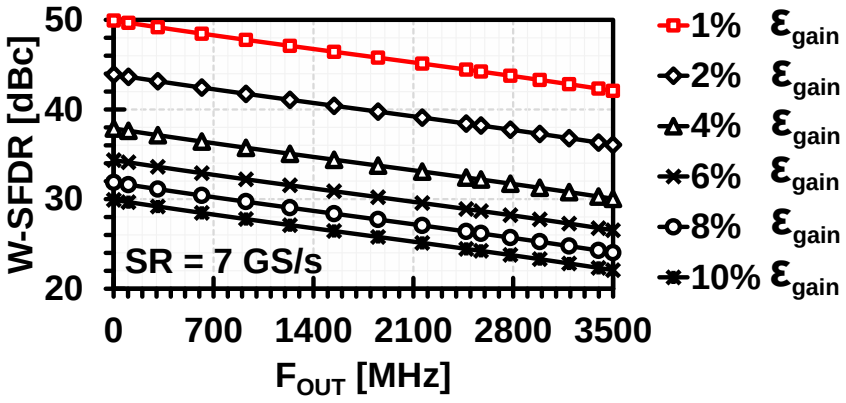


Fig. 2.6. Gain mismatch error profiles.

Where:

- F_{OUT}: Frequency of the output signal.
- Δt: Sampling time error.

$$W\text{-}SFDR = 20\log_{10}\left(\frac{1}{\pi \cdot F_{OUT} \cdot \Delta t}\right) \tag{2.4}$$

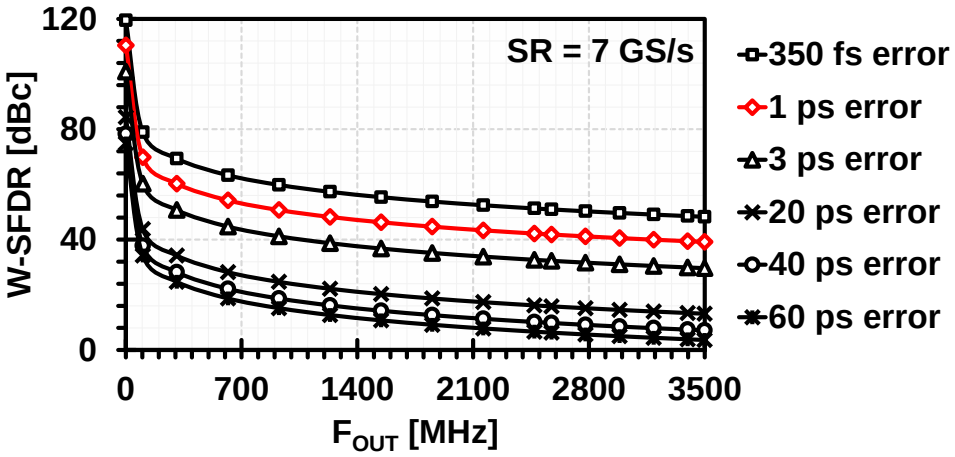


Fig. 2.7. Duty cycle error profiles.

$$SNR_{\Delta t} = 20\log_{10}\left(\frac{1}{2\pi \cdot F_{OUT} \cdot \Delta t}\right) \tag{2.5}$$

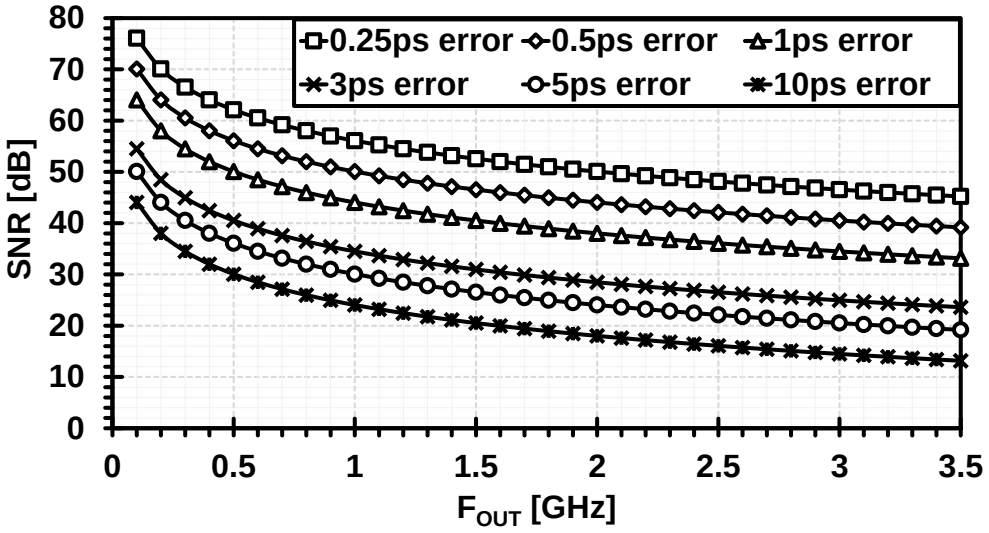


Fig. 2.8. SNR degradation due to clock jitter.

2.4 High-speed CMOS-friendly two-times interleaved RDAC

In this work, a two-times interleaving RDAC (2I-RDAC) is proposed (Fig. 2.9) and integrated with a complementary dual-phase latch-based NCO core. This architecture results in a complete-DDFS-solution capable of generating two samples per clock cycle. The proposed converter comprises two digital signal processing functional units (DSP_A/DSP_B) divided into mirrored layers (ODD/EVEN) having a phase offset of 180° between the active levels of equivalent sequential elements.

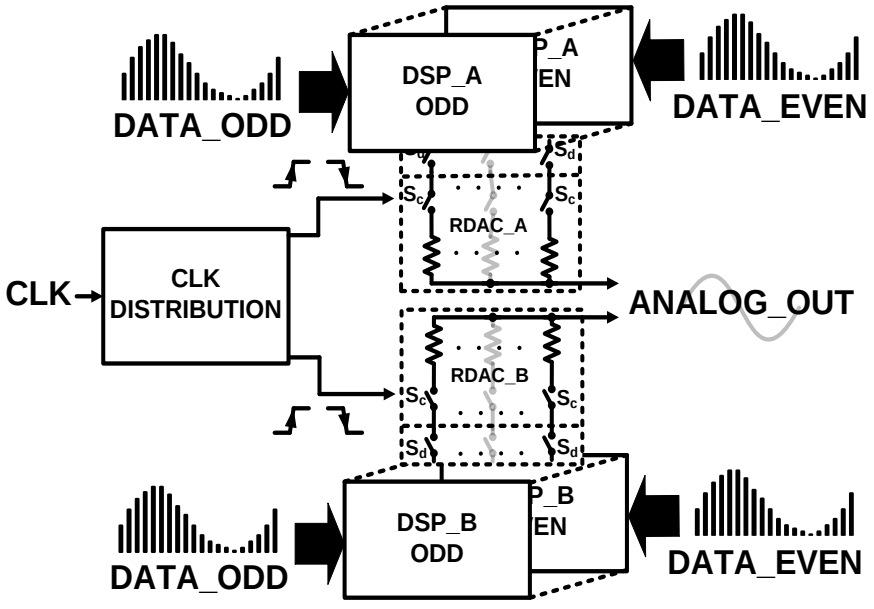


Fig. 2.9. General architecture of the proposed interleaved RDAC.

A code-dependent switching stage (S_d) connects a differential resistive array (RDAC_A-RDAC_ B) either to V_{DD} (1.2V) or V_{SS}. The access to the V_{OUTP} and V_{OUTN} outputs is arbitrated by a row of interleaving switches enabled by *CLK*. These switches will alternate the digital outputs from the DSP_A and DSP_B during different levels of the reference clock. This design exhibits three key advantages when compared with previously reported DACs employing interleaving architectures. First, when using the proposed resistor-based topology, the output impedance becomes code-independent. Second, unlike in current-steering based DACs, a rail-to-rail operation can be achieved even under the limited voltage headroom conditions imposed by the continuous technology scaling.

Finally, by sharing in time a common resistor array among the interleaved digital logic, the system becomes more robust against the inter-DAC gain and offset effects. The ε_{gain} can be reduced in (2.3) by sharing a common resistor array between the two complementary DSP units in Fig. 2.9 (only the data and interleaving switches are not shared). Thus, the main source of the undesired spurs mechanism can be effectively mitigated. Note that the DATA_ODD and DATA_EVEN signals are processed in both DSP_A and DSP_B units in Fig. 2.9. In other words, these complementary inputs share in time the whole differential resistor array (RDAC_A + RDAC_B) and will always generate an output signal that is equally affected by any mismatch between the resistors in the single-ended paths. However, since the last interleaving stage is controlled by the clock signal, the skew and duty-cycle balance are still critical factors.

2.5 Dynamic element matching techniques

Different methods have been proposed in order to reduce the non-linear distortions due to element mismatches in the DACs [57], [58]. Data weighted averaging (DWA) have been commonly employed in oversampling applications [57] meanwhile randomized thermometer-coding (RTC) method has been reported in Nyquist-rate DACs [58]. Although in both cases SFDR improvements can be achieved by suppressing the mismatch effects, the switching activity is increased compared with a thermometer-coded converter [55]. The random swapping thermometer coding dynamic element matching (RSTC-DEM) was proposed by Shen et al. in [55]. This method is capable of suppressing the distortions caused by the device mismatches while keeping the glitch energy at the levels of a thermometer coded converter. This is a very important feature for high-speed data converters in which the dynamic distortions commonly dominates the SFDR performance. However, up to date, the application of

this method has been limited to low-speed systems (≤ 200MS/s) [59]. Table 2-2 summarizes the described differences among previously reported DEM methods according to the simulation results disclosed in [55]. In this work, the RSTC-DEM will be adopted to improve the SFDR performance of the complete-DDFS-solution and digital optimization techniques will be introduced in order to increase the throughput of the DEM core.

TABLE 2-2: COMPARISON OF SEQUENCING ELEMENTS.

Encoding	Glitch [pV-s]	Noise shaping	Application
Thermometer	0	No	High-speed DAC
RTC [58]	7.3	No	Nyquist-rate DAC
DWA [57]	6.4	Yes	Oversampling DAC
RSTC-DEM [55]	0	No	Low-speed DAC

2.6 Summary of the design methodology for high-speed CMOS-based DM-DDFS

In summary, the design methodology for high-speed DDFS presented in this chapter is based on five premises (Fig. 2.10). First, it is recommended to adopt a digital-intensive architecture like the DM-DDFS in order to be able to implement the FM+PM+AM capabilities and take advantage of the CMOS technology scaling benefits. Second, PA and PAC blocks with feed-forward topologies are preferred in order to optimize them by using pipelining and parallel structures in a fully synthesizable flow. Third, implementing these digital blocks by employing the complementary dual-phase latch based method seems to be an effective approach given the benefits in terms of timing performance, area, power consumption and yield. Next, a rail-to-rail operation can be achieved even under the limited voltage headroom conditions along with the continuous technology scaling by integrating a two-times interleaved RDAC. This is an important feature in terms of technology portability. Also, the output impedance becomes code independent, eliminating the distortions originated by the output impedance modulation effects in current-steering DACs. Finally, the distortions arising from the mismatch among the resistive units can be reduced without increasing the switching activity in the RDAC cells by employing the RSTC-DEM method. The combination of these techniques results in a CMOS-friendly architecture that can increase the system throughput by generating two samples per clock cycle with a rail-to-rail voltage swing.

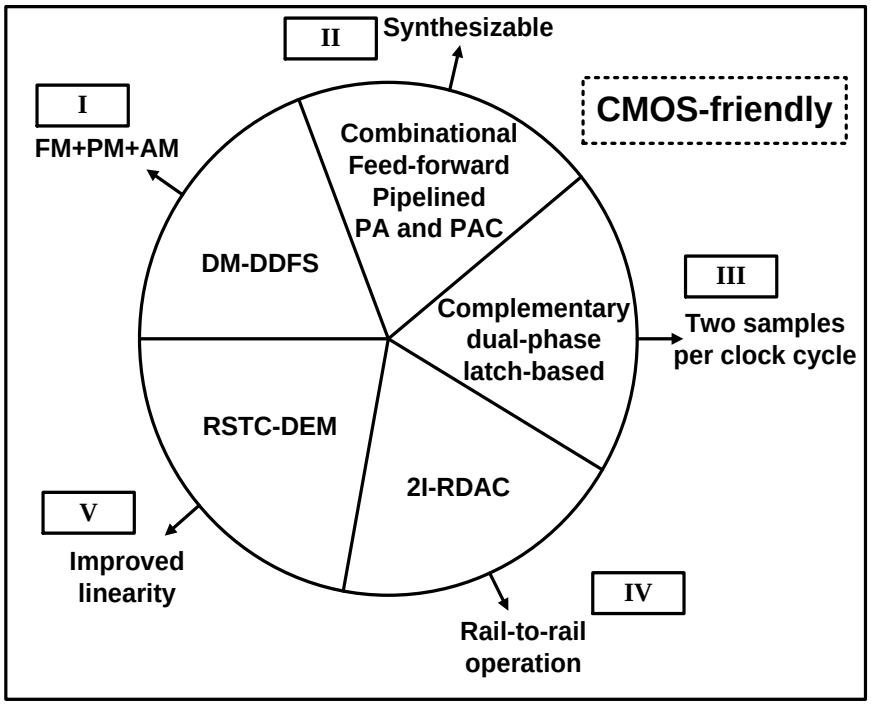


Fig. 2.10. High-speed design methodology for CMOS-based DDFS.

CHAPTER 3:
COMPLEMENTARY DUAL-PHASE LATCH-BASED NCO

THE block diagram of the proposed NCO core is illustrated in Fig. 3.1. The complementary dual-phase latch-based sequencing method is employed in the timing critical modules (PA and PAC) [60].

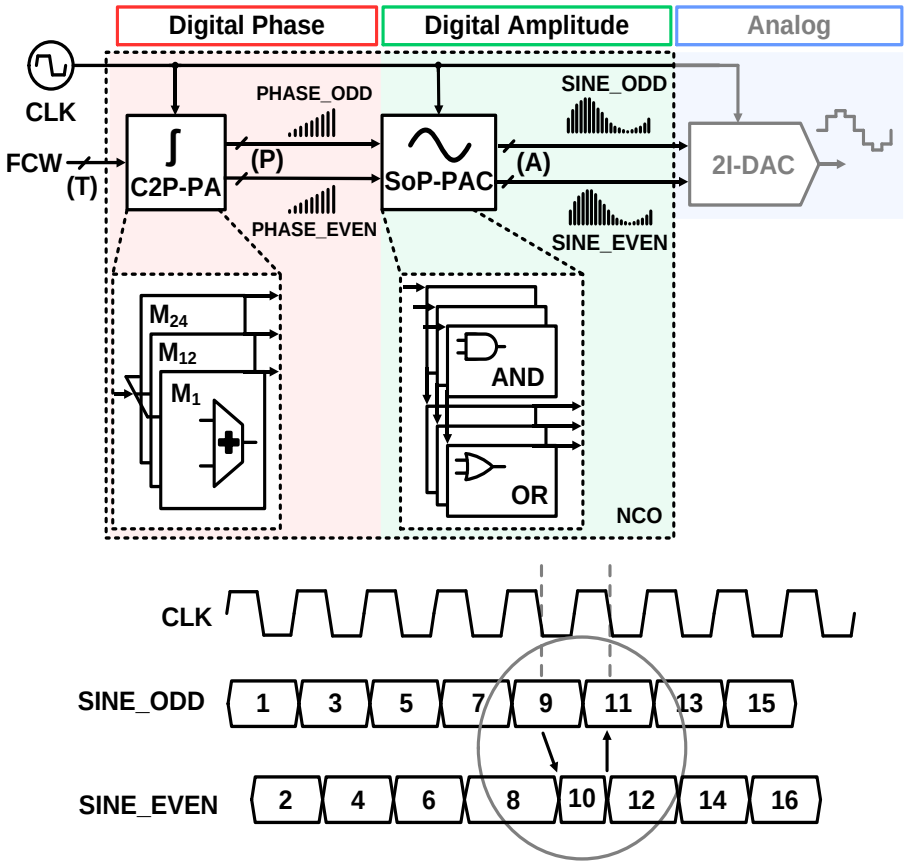


Fig. 3.1. Proposed NCO general architecture and timing diagram.

Where:

- Tuning word length (T) = 24 bits.
- Phase word length (P) = 14 bits.

- Amplitude word length (A) = 10 bits.

A 24-bits complementary dual-phase latch-based phase accumulator (C2P-PA) that generates two samples per clock cycle was implemented in the digital phase domain. A dual-phase, sum of product terms based, phase to amplitude converter (SoP-PAC) that can match the speed of the C2P-PA by using a feed-forward topology is introduced in the digital amplitude domain. This architecture can be used in combination with two parallel DAC cores operating alternatingly (two-times interleaved DAC (2I-DAC)). The analog performance requirements can be relaxed when using this structure because each DAC will operate at one-half of the sampling rate. The *SINE_ODD* and *SINE_EVEN* output data need to be aligned before the DAC input in order to avoid potential glitches caused by the borrowed time in the NCO core. The theoretical limits of the phase truncation SFDR and the SNR can be calculated from (1.2) and (1.4) as follows [60]:

$$SFDR = 6.02 \times 14\, dBc = 84.28\, dBc \tag{3.1}$$

$$SNR = 6.02 \times 10 + 1.76\, dB = 61.96\, dB \tag{3.2}$$

This topology trades-off area and power efficiency when compared to non-parallel flip-flop-based architectures. Its main drawback is a larger area occupation because of the duplicated combinational logic in the complementary dual-phase latch-based PA and PAC blocks. Furthermore, the clock tree complexity proportionally scales with the increased amount of sink cells (complementary latch pairs). This also leads to a higher consumption of routing resources. However, this design exhibits two key advantages compared with previously reported DDFSs employing parallel architectures [61] [62]. First, the system speed can be increased by exploiting the time borrowing property. The period limitation imposed by the strict timing constraints in flip-flop-based parallel architectures can be overcome. Consequently, the power efficiency can be also improved. Second, although the combinational logic in both cases is duplicated, area can be saved when using latches as synchronizing elements instead of flip-flops. Note that this reduction depends on the size ratio between the latch and flip-flop standard-cells for a given technology library (section 2.1) [60].

The maximum output frequency can be doubled by introducing the complementary dual-phase latch-based sequencing method into a DM-DDFS architecture. New sinusoidal samples can be generated on both high and low levels of the clock. The modified tuning equation results as follows [60]:

$$F_{OUT} = \frac{FCW \cdot F_{CLK}}{2^{\text{T-1}}} \tag{3.3}$$

It can be noticed that, under the same conditions (*FCW*, F_{CLK} and *T*), the maximum output frequency is doubled when compared with (1.1). This design features a pipelined PA module comprising 24 complementary dual-phase latch-based phase accumulators (M_1 to M_{24} in Fig. 3.1). The outputs of the PA block are the complementary phase ramps *PHASE_ODD* and *PHASE_EVEN*. These signals are active during different levels of the clock and used as reference information for the sinusoidal samples generation in the PAC. The logic is represented in the form of SoP terms obtained from a 14×10-bits sinusoidal lookup table. The product terms are placed into the first pipeline stage because they are the slowest combinational logic (AND blocks in Fig. 3.1). Successive stages are only composed of two-input OR gates (OR blocks in Fig. 3.1). This allows to borrow time, optimize the critical paths of the SoP terms and reduce delay costs. Even though the transition from data number 8 to 10 occurs after the falling edge of the clock *CLK* in Fig. 3.1, the extra delay can be allocated in the next half cycle. The amount of borrowed time depends on the combinational logic delay associated with data 10, the setup time for the given technology and the clock skew. Equation (3.4) is derived from (2.2) and represents the special case when there is a combinational logic delay after the second latch in the complementary dual-phase latch-based sequencing pair [60]. The C2P-PA and SoP-PAC structures will be discussed in next sections.

$$T_{b\_data8} = T_{clk/2} - \left(T_s + T_{skew} + T_{data10}\right) \tag{3.4}$$

Where:

- T_{b_data8}: Time borrowed by data 8 related logic.
- $T_{clk/2:}$ Half clock period.
- T_{data10}: Data 10 propagation delay.

3.1 24-bits complementary dual-phase latch-based phase accumulator

3.1.1. Issues of high-speed phase accumulators

Conventionally, pipelined phase accumulators are employed in high-speed applications (Fig. 3.2) [4]. However, this architecture trade-off speed with area and latency. The flip-flop area increases exponentially and the adder logic area increases

linearly with the number of input bits (N) and truncated output bits (M) [63]. Similarly, the latency is directly proportional to N.

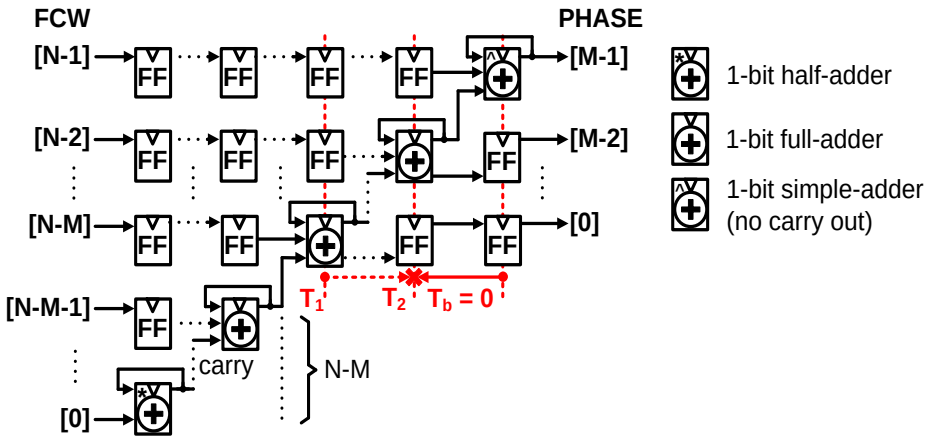


Fig. 3.2. Conventional pipelined phase accumulator.

$$A_{ACC\_FF} = \frac{\left(N^2 + 5N\right) + \left(M^2 - M\right) - 2}{2} \cdot A_{FF} + NA_{ADDER} \tag{3.5}$$

$$L_{FF} \propto N \tag{3.6}$$

Where:

- A_{CC_FF}: Area of the flip-flop based pipelined accumulator.
- N: Input word length.
- M: Truncated output length.
- A_{FF}: Flip-flop area.
- A_{ADDER}: Area of the adder logic (accumulator mode).
- $L_{FF:}$ Latency of the flip-flop based pipelined accumulator.

Another limitation resides in the fact that the adder logic delay is strictly constrained to one clock period when flip-flops are used. Even though in the post-skewing pipeline stages no logic operation is executed, all the calculations need to be finished within the clock period starting from the edge that triggers the adder logic. As an example, in Fig. 3.2, the signal propagating from point T_1 through the accumulator unit needs to settle strictly before the rising edge in the receiving flip-flop (point T_2). Hence, no time can be borrowed between consecutive stages (T_b=0).

3.1.2. Complementary dual-phase latch-based phase accumulator

This solution is based on a parallel architecture synchronized by using the complementary dual-phase latch based method (Fig. 3.3). The equation of the resulting equivalent area can be estimated from (3.7)-(3.9). Even though a mirrored structure is used and the number of cells is duplicated, the area penalty is relatively small because the latches of the employed technology have about 57% of the equivalent flip-flop size (3.8) (section 2.1). The resulting area in terms of equivalent flip-flops count is plotted against *N* in Fig. 3.4.

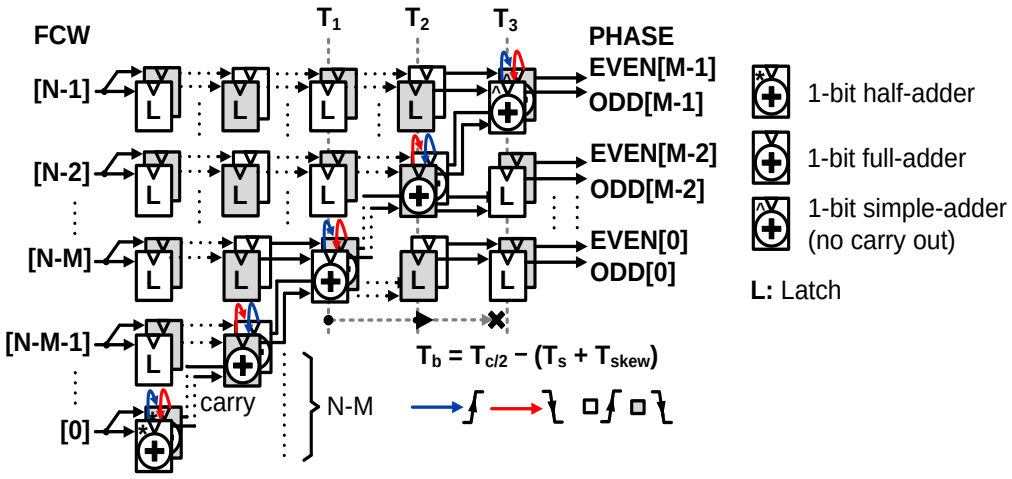


Fig. 3.3. Complementary dual-phase latch-based phase accumulator**.**

$$A_{ACC} = 2 \cdot \frac{\left(N^2 + 5N\right) + \left(M^2 - M\right) - 2}{2} \cdot A_L + 2NA_{ADDER} \tag{3.7}$$

Since:

$$A_L \approx 0.57 A_{FF} \tag{3.8}$$

Then:

$$A_{ACC\_L} = \left(\left(N^2 + 5N\right) + \left(M^2 - M\right) - 2\right) \cdot 0.57 A_{FF} + 2NA_{ADDER} \tag{3.9}$$

Where:

- A_{CC_L}: Area of the latch-based pipelined accumulator.
- A_L: Latch area.

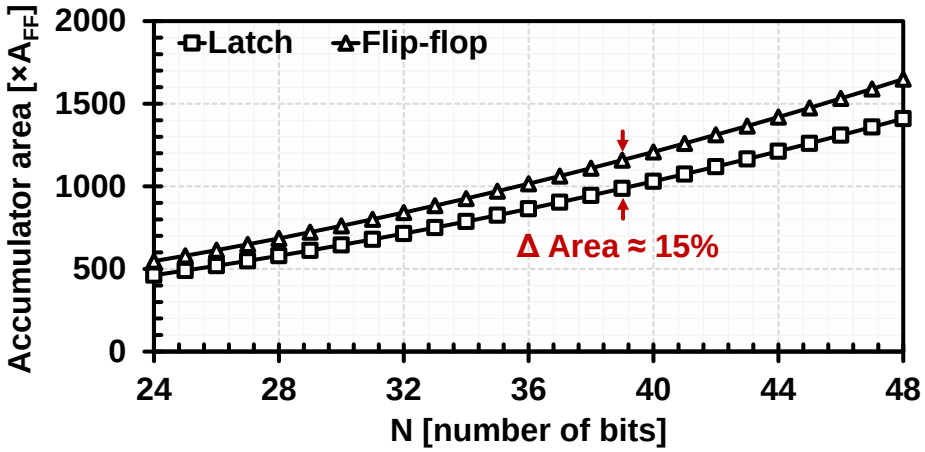


Fig. 3.4. Normalized area vs. accumulator size.

The number of input bits was changed from 24 to 48 (typical accumulator length in DDFS applications). The length of M was kept constant (14 bits) by also increasing the number of truncated bits in unary steps from 10 bits to 34 bits. The area of the latches was assumed to be 57% of the equivalent flip-flop size. Similarly, the proportions of the adder logic (A_{ADDER}) was assumed to be equal to the flip-flop dimensions. These values resemble the size relationship among the cells in the employed standard cell library. It should be noticed that the area penalty is never larger than 20% of the flip-flop based design. Moreover, the accumulator latency is halved because two samples are generated within one clock cycle (3.10). Also, since the latches are transparent devices, the logic delay in the adder units can be "spread" among the post-skewing pipeline stages by using the time borrowing property. This is represented in Fig. 3.3 as a dashed line starting in point T_1, passing through T_2 and ending before the next receiving latch (T_3).

$$L_L \propto \frac{N}{2} = \frac{L_{FF}}{2} \tag{3.10}$$

As previously mentioned, the C2P-PA comprises 24 complementary dual-phase latch-based 1-bit phase accumulators. Each of these logic units is based on parallel 1-bit adder cells operating in complementary mode (Fig. 3.3). This PA can be considered as a pipelined ripple-carry accumulator active during both levels of the clock *CLK* (Fig. 3.1). It requires a pair of half-adder cells (M_1), forty-six full-adder cells (M_2-M_{23}), two simple-adder cells (M_{24}) (Fig. 3.1) and pre-skewing/post-skewing complementary latches (Fig. 3.3). It exhibits a latency of 12½ clock periods resulting from 25 interleaving operations. The complementary transitions among the sum outputs are represented as colored lines in Fig. 3.3. It should be noted that these signals are

post-skewed as well as interleaved among the adder cells in order to perform the complementary accumulation operations. The worst case propagation delay is limited to only 1-bit full-adder plus the sequencing overhead of the employed latches. A detailed view of a 2-bits C2P-PA is shown in Fig. 3.5 and can be employed to illustrate the logic operation. M_1 and M_2 blocks operate in parallel. Complementary latch pairs are used at the input of each M module (L_1-L_2 and L_9-L_{10}) to sample the data [60]. The FCW is updated during both high and low levels of the clock CLK. During the first pipeline stage (P_1) M_1 block samples the $FCW<0>$ data, computing both the arithmetic sum and carry out values. At this time, sum and carry out signals are ready to be sampled during the P_2 stage. Concurrently, M_2 module pipelines the $FCW<1>$ input data to be used during next pipeline stage P_2. During P_2 time window, M_1 block samples the previously calculated carry out and the feedback input for next phase. In parallel, M_2 samples the pipelined data from its own P_1 stage. The output of this step is the arithmetic sum of the second bit. During P_3 stage, M_2 feedbacks the input value to be used during the next phase. Finally, both modules pipeline its input data in order to align the $PHASE\_EVEN$ and $PHASE\_ODD$ outputs. M_1 module comprises two 1-bit half-adder circuits (Fig. 3.6 a)) employed to calculate the arithmetic sum (S) and carry out ($CARRY\text{-}O$) values of the FCW least significant bit (LSB). In this first stage, there is no carry-in (CI) information and the associated hardware can be saved. Similarly, M_2 module employs two 1-bit simple-adder circuits (Fig. 3.6 b)). This module corresponds to the block M_{24} in Fig. 3.1 (24-bits accumulator). This is the final stage and no carry-out information is needed, only the arithmetic sum is implemented.

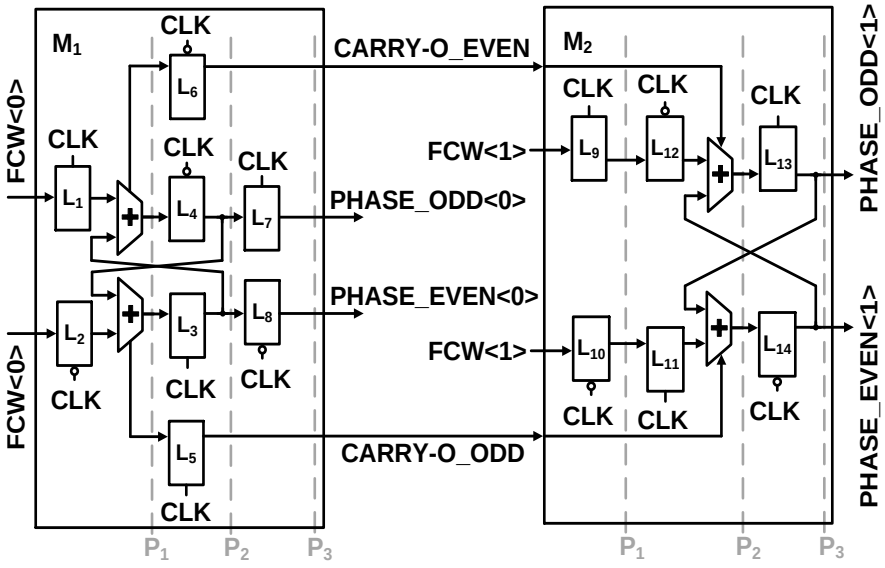


Fig. 3.5. 2-bits complementary dual-phase latch-based phase accumulator.

All inner modules employ 1-bit full-adder circuits (Fig. 3.7) to calculate both the carry-out information and arithmetic sum. The proposed architecture allows doubling the data sampling rate by using the complementary dual-phase latch-based sequencing method and intensive pipeline. This architecture is highly flexible and can be easily extended to an *N*-size phase accumulator by adding (*N* + 1) pipeline stages and *N* parallel *M* modules [60]. The number of registers required in a 24-bits flip-flop based accumulator can be estimated as 438 units from (3.5). The total dynamic power consumption of the register cells follows a distribution with μ = 31.29μW and σ = 3.08μW when running at 3.54GS/s (3.54GHz clock) (Fig. 3.8). A total of 876 latches are needed when using the complementary dual-phase latch-based method (3.9).

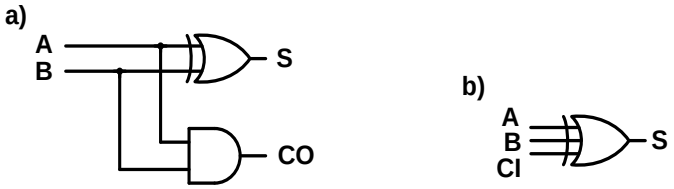


Fig. 3.6. Half-adder and simple-adder circuits.

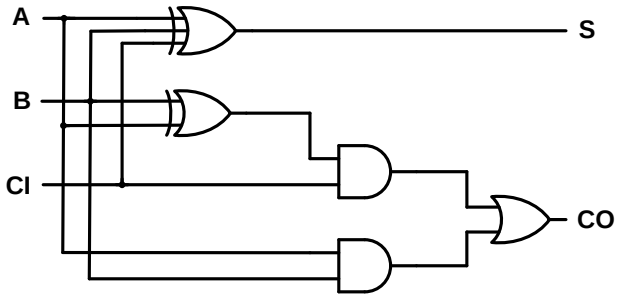


Fig. 3.7. Full-adder circuit.

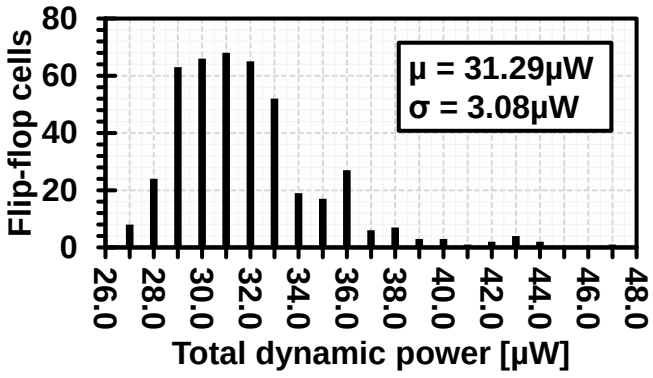


Fig. 3.8. 24-bits flip-flop based phase accumulator. Dynamic power distribution of individual registers when running at 3.54GS/s.

The power consumption follows a considerably more efficient distribution with μ = 3.41μW and σ = 0.68μW when operating at 3.54GS/s (1.77GHz clock) (Fig. 3.9). The mean value becomes μ = 7.40μW and the standard deviation reaches σ = 1.48μW when increasing the sampling rate up to 7.6GS/s (3.8GHz clock) (Fig. 3.10). The power breakdown of the 24-bits PAs employing flip-flops and latch cells are represented in Fig. 3.11 and 3.12 respectively. It should be noticed how the dominant contribution comes from the internal power of the registers in Fig. 3.11. The power dissipated in the clock tree structure become dominant in the C2P-PA case (Fig. 3.12). The post-layout simulation results demonstrate the merits of the discussed high-speed accumulator (Fig. 3.13). It can achieve more than twice the sampling rate while having a comparable power consumption with an area penalty of about 25%. The extra area (about 10% when compared with the estimated results in Fig. 3.4) is needed to allocate the more complex signal routing and the clock tree structure.

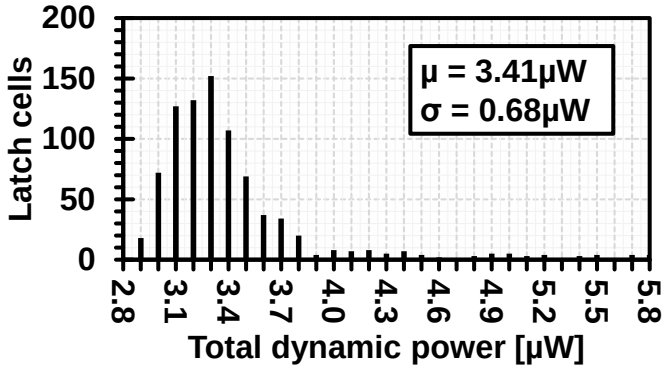


Fig. 3.9. 24-bits complementary dual-phase latch-based phase accumulator. Dynamic power distribution of individual registers when running at 3.54GS/s.

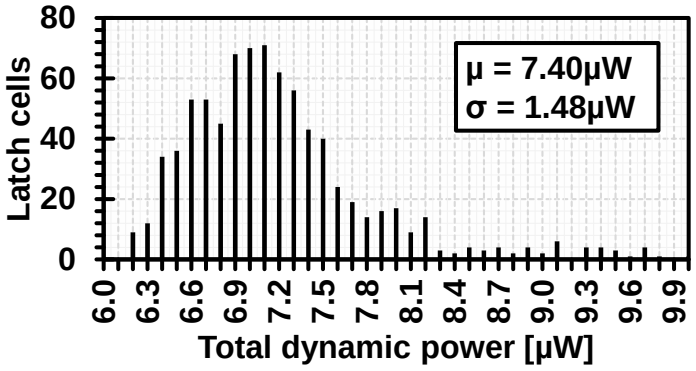


Fig. 3.10. 24-bits complementary dual-phase latch-based phase accumulator. Dynamic power distribution of individual registers when running at 7.6GS/s.

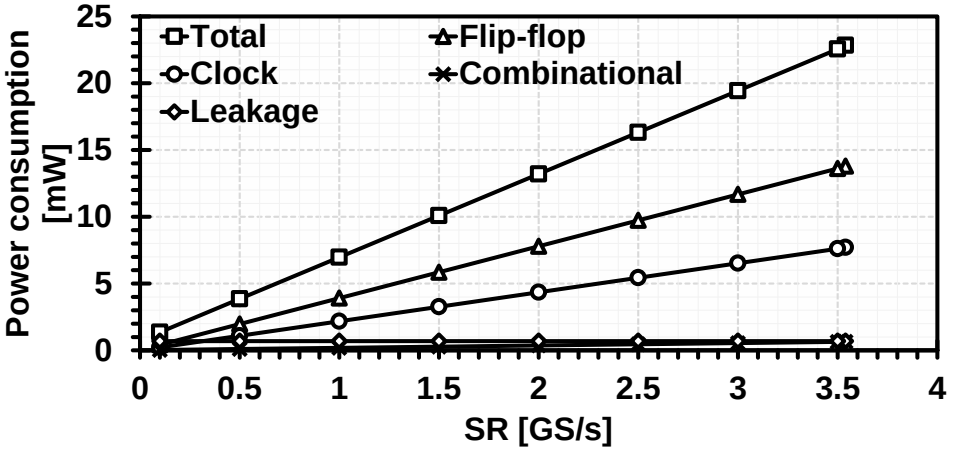


Fig. 3.11. Power breakdown. 24-bits accumulator. Flip-flop based architecture. 3.54GS/s.

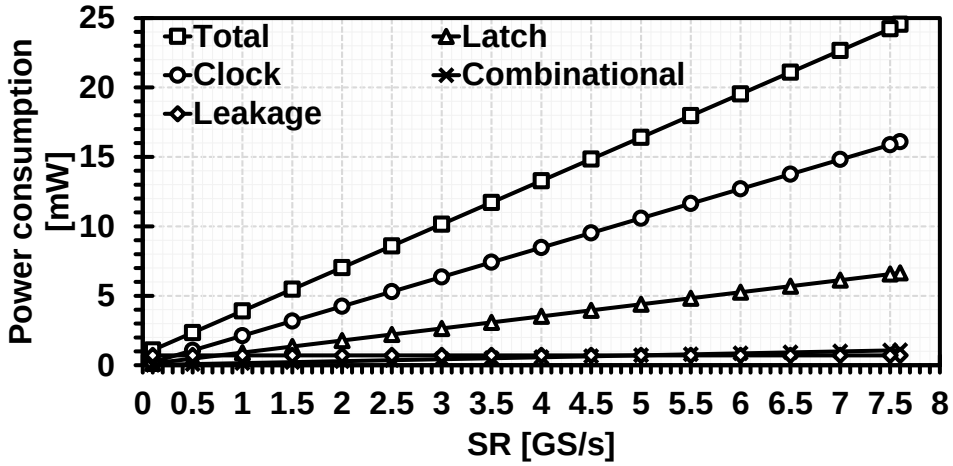


Fig. 3.12. Power breakdown. 24-bits accumulator. Latch-based architecture. 7.6GS/s.

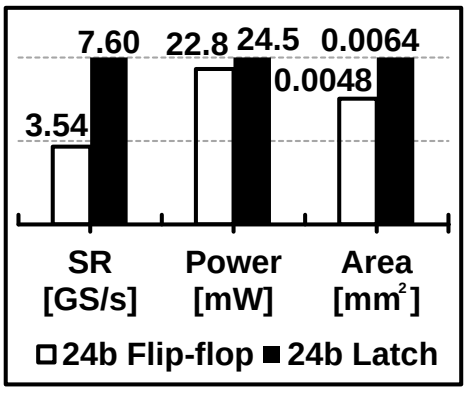


Fig. 3.13. Post layout simulation results.

3.2 Dual-phase sum of product terms based phase to amplitude converter

The SoP-PAC technique was implemented in the digital amplitude domain and consist of three basic steps (Fig. 3.14). To begin, the first quarter of a sine waveform is mapped from a 14×10-bits sinusoidal lookup table into SoP terms. Second, the logic structure is pipelined by using the complementary dual-phase latch-based method. And finally, since the sine waveform has the symmetry property, the remaining quarters can be generated by using the quarter wave symmetry (QWS) technique [2]. A 6.8GS/s operation can be achieved by simulation [60]. Any boolean function can be written in a canonical form by only using AND, OR and NOT functions [52]. This basic idea can be applied to replace the power-hungry and area consuming sinusoidal lookup table by a purely combinational circuit in the digital mapping architecture. As an example, the SoP term corresponding to the *SINE_ODD<8>* and *SINE_EVEN<8>* outputs is represented in (3.11). The product terms (*A1* to *A5*) are placed into the first pipeline of the array because they are the slowest combinational logic. In this way, time can be borrowed in order to optimize critical paths and reduce delay costs. Successive stages are only composed of two-input OR gates. The complexity of the generated hardware increases towards the least significant bit (LSB). Since the generated SoP terms contain more than one OR operation, 11 pipeline stages were added (P_2-P_{12} in Fig. 3.14).

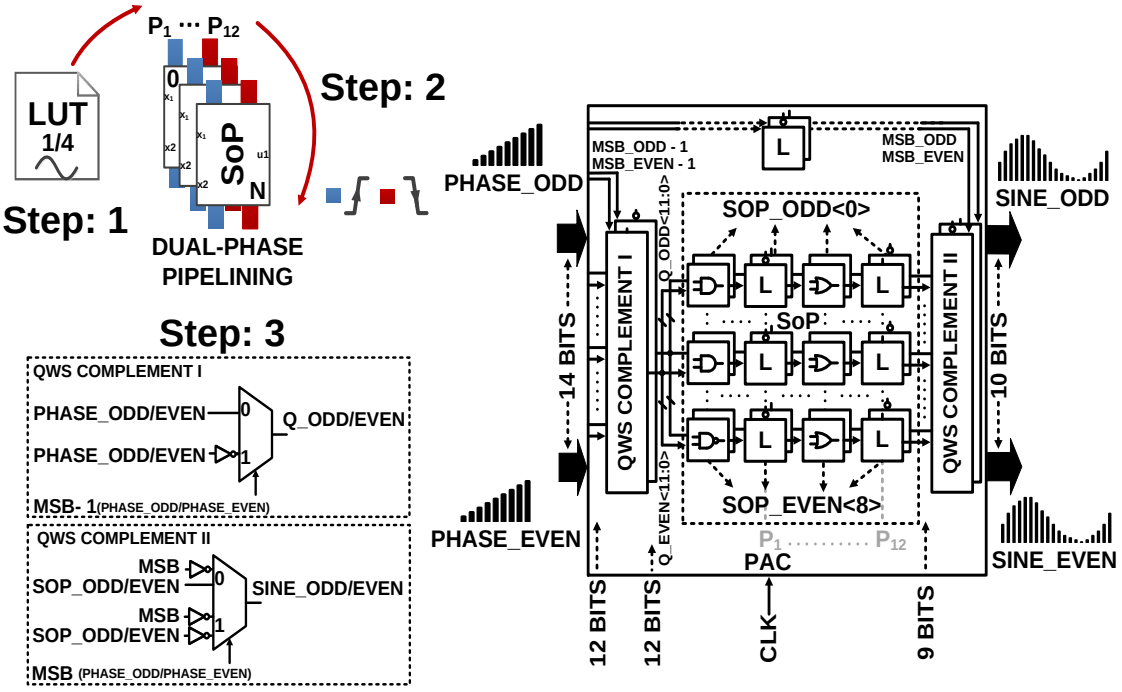


Fig. 3.14. SoP-PAC technique design flow.

$$
\begin{aligned}
&SOP\langle 8\rangle = Q\langle 11\rangle \; OR \; (A1, A2, A3, A4, A5) \\
&A1 = AND \; (NOT \; Q\langle 11\rangle, Q\langle 10\rangle, Q\langle 9\rangle) \\
&A2 = AND \; (NOT \; (Q\langle 11\rangle, Q\langle 9\rangle), Q\langle 10\rangle, Q\langle 8\rangle, Q\langle 7\rangle) \\
&A3 = AND \; (NOT \; (Q\langle 11\rangle, Q\langle 9\rangle, Q\langle 7\rangle), Q\langle 10\rangle, Q\langle 8\rangle, Q\langle 6\rangle, Q\langle 5\rangle) \\
&A4 = AND \; (NOT \; (Q\langle 11\rangle, Q\langle 9\rangle, Q\langle 7\rangle, Q\langle 5\rangle), Q\langle 10\rangle, Q\langle 8\rangle, Q\langle 6\rangle, Q\langle 4\rangle, Q\langle 3\rangle) \\
&A5 = AND \; (NOT \; (Q\langle 11\rangle, Q\langle 9\rangle, Q\langle 7\rangle, Q\langle 5\rangle, Q\langle 3\rangle), Q\langle 10\rangle, Q\langle 8\rangle, Q\langle 6\rangle, Q\langle 4\rangle, Q\langle 2\rangle, Q\langle 1\rangle)
\end{aligned}
\tag{3.11}
$$

The equivalent logic circuit can be easily speeded up by using complementary dual-phase latch-based sequencing method in a pipelined architecture. In summary, this system can be entirely made up of combinational logic inserted into 12 complementary dual-phase latch-based pipeline stages (Fig. 3.14) [60]. To the best of our knowledge, this approach has not been reported in any previous high-speed DDFS design. Lastly, since only one quadrant of the sine needs to be stored (sine has the symmetry property), the size of the memory can be reduced by more than 75% [2]. By numerically flipping the 1^{rst} quarter of the sinusoid in the order indicated in Fig. 3.15 (1 → 2 → 3 → 4), the full cycle can be generated without incurring any associated error. The 2nd, 3rd and 4th quadrants of the sine waveform are generated by using the quarter wave symmetry technique. The extra circuit needed for the QWS quadrant generation is simple and can be inserted into the pipeline array. The logic of the compression algorithm is divided into two segments: QWS COMPLEMENT I and QWS COMPLEMENT II (Fig. 3.14). In both cases, the complementary dual-phase latch-based sequencing method was employed in order to speed up the timing performance. The former one multiplexes the inverted and non-inverted *PHASE_X<11:0>* signals depending on the *MSB_X-1* corresponding value. The suffix *X* refers to the complementary *EVEN* or *ODD* signals in all cases.

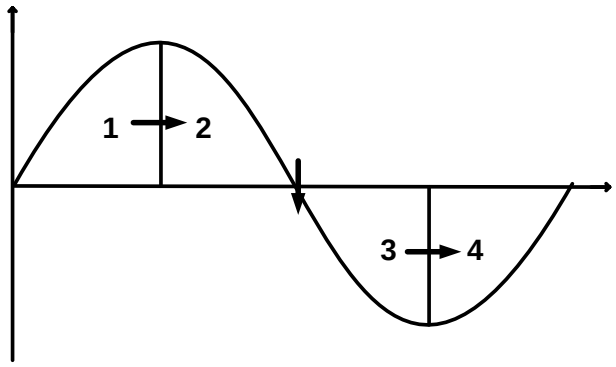


Fig. 3.15. Quarter wave symmetry technique.

In this way, the vertical flip operations 1→2 and 3→4 in Fig. 3.15 can be implemented. The second block mirrors the data about the horizontal axis in order to generate the full sine waveform period. The *MSB_X* is pipelined and used as reference information when multiplexing the *SOP_X <8:0>* signal and its complement as represented in Fig. 3.14. An inverted version of the *MSB_X* is employed as the *SINE_X <9>* output to the DAC. Consequently, only the SoP terms of the remaining 9 LSBs are required [60]. For comparison purposes, a flip-flop based SoP-PAC was initially designed and simulated. The total number of registers is 3470 after pipelining with flip-flops the generated SoP terms and QWS blocks. The dynamic performance of the sequencing elements in this reference design follows the distribution in Fig. 3.16 when running at a maximum sampling rate of 3.54GS/s. The equivalent dual-phase sum of product terms based phase to amplitude converter exhibits the dynamic power distribution in Fig. 3.17 when running at 3.54GS/s (1.77GHz) (total latch count = 6940).

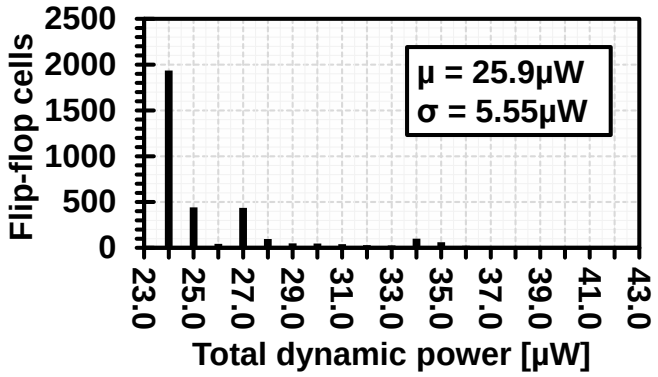


Fig. 3.16. Flip-flop based SoP-PAC. Dynamic power distribution of individual registers when running at 3.54GS/s.

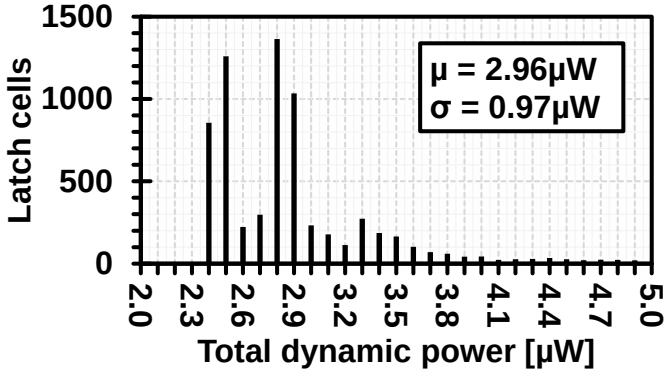


Fig. 3.17. Latch-based SoP-PAC. Dynamic power distribution of individual registers when running at 3.54GS/s.

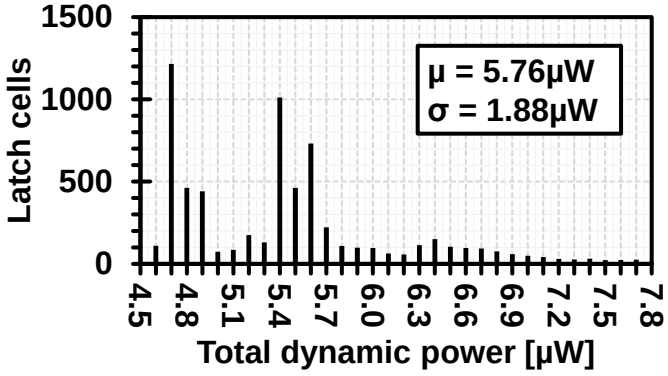


Fig. 3.18. Latch-based SoP-PAC. Dynamic power distribution of individual registers when running at 6.92GS/s.

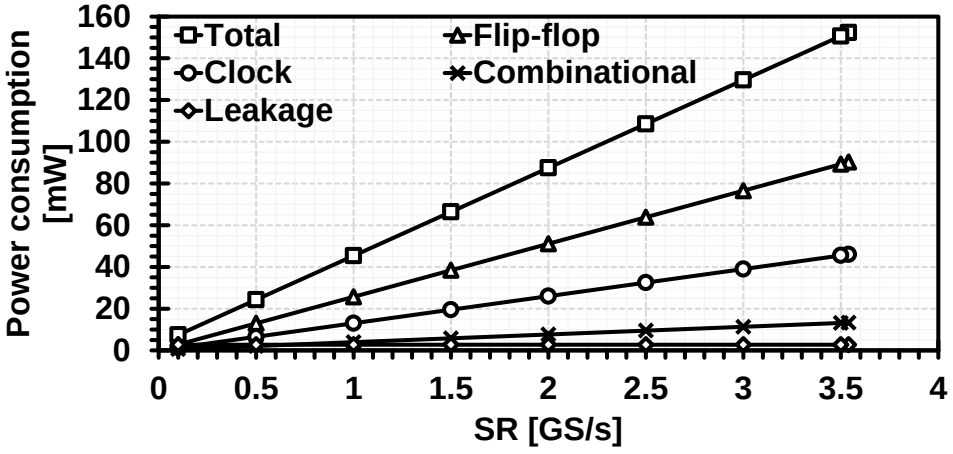


Fig. 3.19. Power breakdown. SoP-PAC. Flip-flop based architecture. 3.54GS/s.

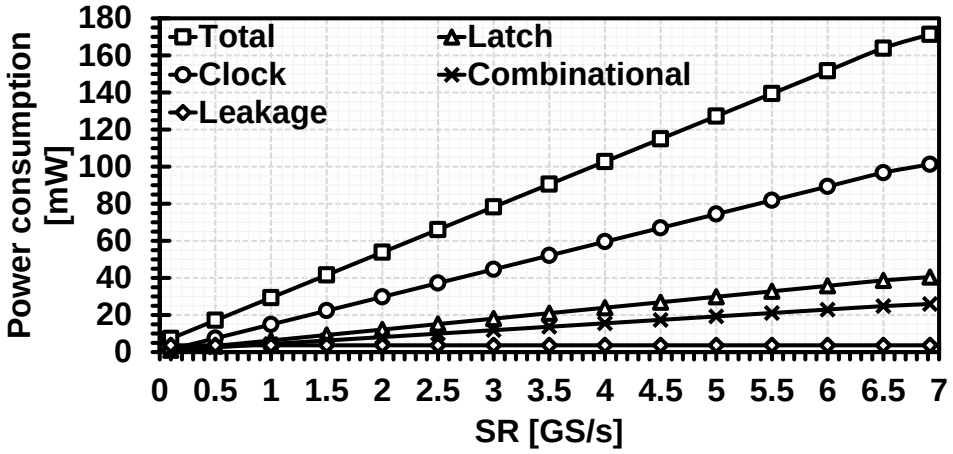


Fig. 3.20. Power breakdown. SoP-PAC. Latch-based architecture. 6.92GS/s.

The median value becomes μ = 5.76μW and σ = 1.88μW when increasing the sampling rate up to 6.92GS/s (3.46GHz clock) (Fig. 3.18). The power breakdowns of

both implementations are represented in Fig. 3.19 and Fig. 3.20. Similar trends to those registered in the phase accumulator are observed. The internal dynamic power of the flip-flops is dominant in Fig 3.19. Conversely, the clock net dissipates most of the energy in the complementary dual-phase latch-based case (Fig. 3.20). The post-layout simulation results demonstrate the merits of the proposed SoP-PAC (Fig. 3.21).

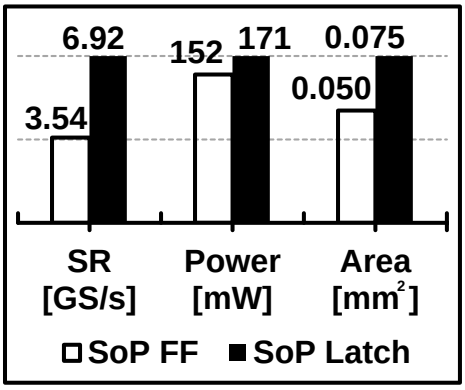


Fig. 3.21. Post layout simulation results. PAC block.

3.3 System implementation

The proposed NCO was designed by using 65nm CMOS, low threshold voltage (LVT), 1.0V, standard-cell library. The RTL design was modeled with Verilog and VHDL description languages and synthesized by employing Synopsys/Design-Compiler tool. Place and route were performed with Synopsys/IC-Compiler. The core size is 0.1mm^2, comprising 25614 cells (Fig. 3.21) [60].

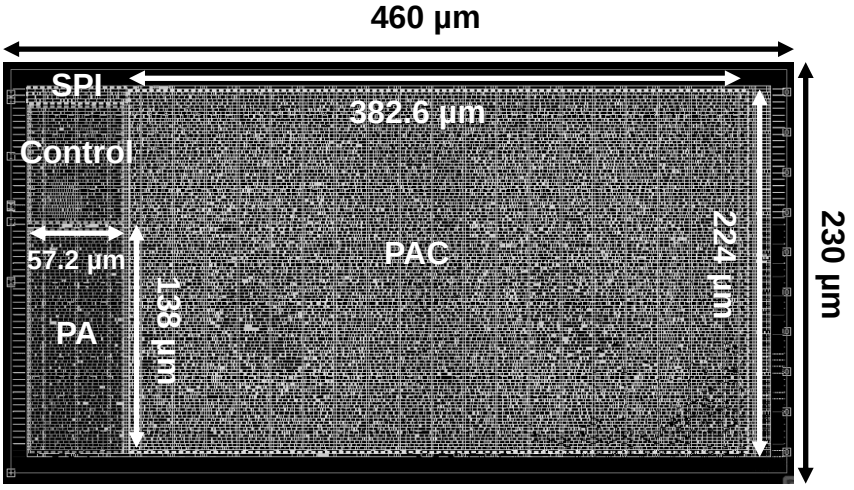


Fig. 3.22. Floorplan view of the proposed NCO.

3.4 Design verification

Static timing, power and area analysis were performed by employing Synopsys/Design-Compiler/IC-Compiler toolset. Behavioral, post-synthesis and post-layout simulation were completed with Mentor Graphics/ModelSim and Cadence/NCsim simulators. Transistor level and SFDR simulations were executed with Cadence/APS.

3.4.1 Static timing, power and area analysis

In ultra-deep submicron designs, interconnect has a major effect on path delays. Accurate estimates of parasitic resistance and capacitance are necessary when targeting high-speed performance. In this work, Design-Compiler topographical mode has been used in order to derive the "virtual layout" of the design. This tool can predict and use more accurate parasitic elements values compared with statistical net approximations based on wire load models. Consequently, the correlation results between post-synthesis and post-layout are improved. Table 3-1 shows the results for static timing, power and area analysis for both post-synthesis and post-layout stages. The increase of the active area after place and route is mainly determined by the tap-cell array insertion (to ensure all standard-cells placed subsequently comply with the maximum diffusion-to-tap distance limit). The presence of clock skew in a complementary dual-phase latch-based system results in unintended time borrowing. Therefore, the max-timing constraint is unaffected if there is enough time headroom to allocate the clock skew. According to static timing analysis results, the maximum time that can be borrowed when running at 6.8GS/s is 100ps. The actual borrowed time is 80ps. As a result, the system can tolerate up to 20ps of clock skew when running at maximum frequency without incurring any max-timing violation. The min-timing constraint linearly depends on the clock skew according to (3.12) [52]. The hold time (T_{hold}) of the latches in the employed 65nm CMOS library is a negative value. Hence, in this case, the minimum delay constraint can be less stringent. According to static timing analysis results, the maximum clock skew which produces no min-timing violations is 60ps.

TABLE 3-1: STATIC TIMING, POWER AND AREA ANALYSIS RESULTS.

	Max F_{CLK} [GHz]	**Sampling rate [GS/s]**	**Active area [mm^2]**	**Power [mW]**
Post-synthesis	3.7	7.4	0.068	150.2
Post-layout	3.4	6.8	0.079	153.2
Correlation (%)	8.1	8.1	13.9	1.9

$$T_{\min} \geq T_h - T_{ccq} + T_{skew} \tag{3.12}$$

Where:

- T_{min}: Minimum propagation delay.

The max-timing constraint limits the worst case clock skew to 20ps. In consonance with (2.2), the maximum time that can be borrowed will increase proportionally with a decrease in the clock frequency (increase in $T_{c/2}$). Correspondingly, for a fixed borrowed time, the system clock skew tolerance will also increase [60].

3.4.2 Behavioral, post-synthesis and post-layout simulation

Fig. 3.23, Fig. 3.24 and Fig. 3.25 show the time domain simulations.

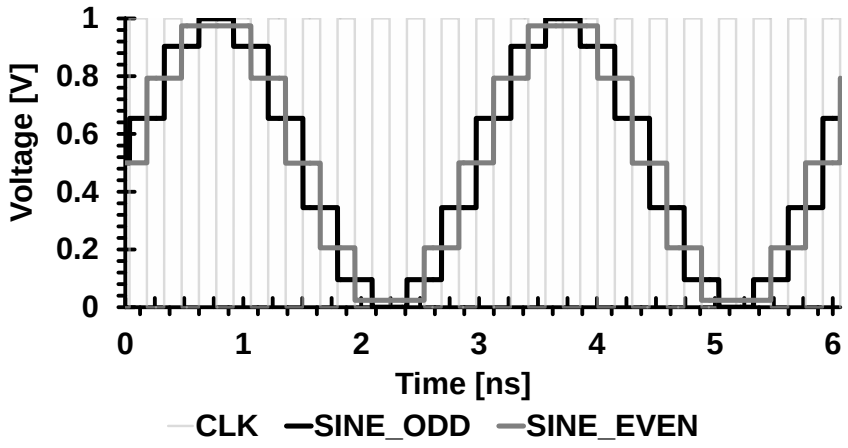


Fig. 3.23. Behavioral simulation. F_{CLK} = 3.4GHz. F_{OUT} = 340MHz.

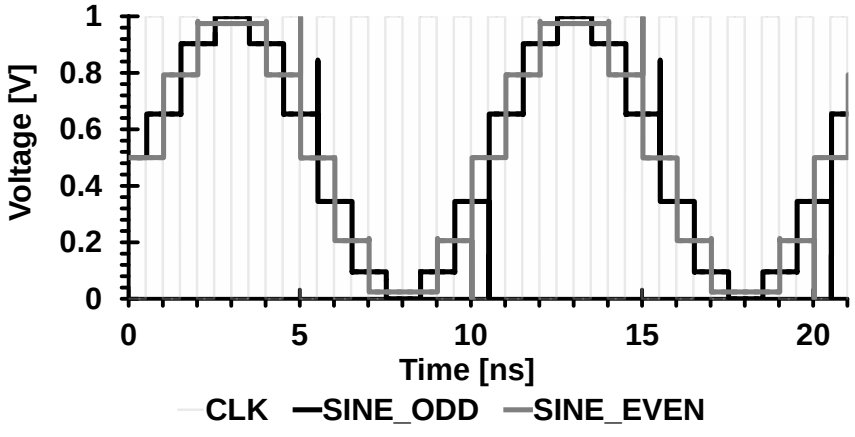


Fig. 3.24. Post-synthesis simulation. F_{CLK} = 1GHz. F_{OUT} = 100MHz.

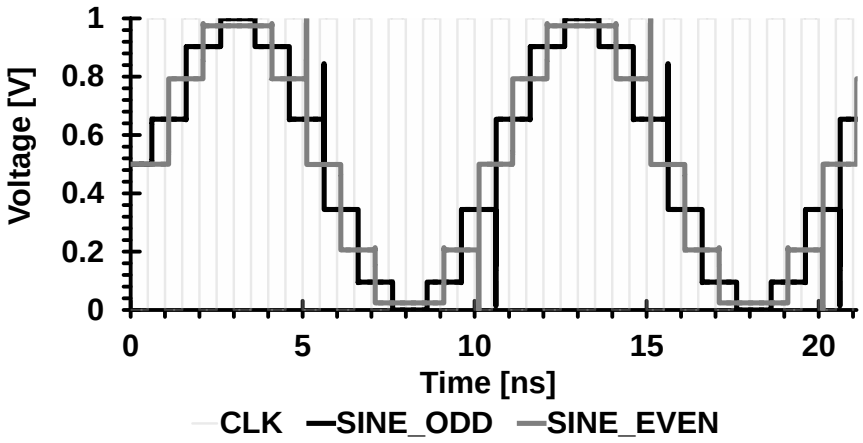


Fig. 3.25. Post-layout simulation. F_{CLK} = 1GHz. F_{OUT} = 100MHz.

Post-synthesis and post-layout back-annotated simulations are limited to 1GHz clock frequency due to a minimum period constraint in the standard-cell library models. From Fig. 3.23 it can be noticed that *SINE_ODD* waveform is updated during the high level of the clock and *SINE_EVEN* during the low level. The final sinusoidal waveform is the envelope resulting when superimposing the *SINE_ODD* and *SINE_EVEN* waveforms [60]. As expected, Fig. 3.24 and Fig. 3.25 waveforms are highly correlated (topographical mode has been used for post-synthesis model). Glitches appear as a result of imbalanced delays and borrowed time within the architecture. The worst condition occurs at middle scale transition when the MSB from the *SINE_ODD* or *SINE_EVEN* signal changes its logic state (Fig. 3.24, Fig. 3.25 and Fig. 3.26). Proper retiming is needed before inputting the data to the DAC in order to minimize these code-dependent glitches at the analog output. This can be done by using flip-flops to resynchronize the data at the input of each sub-DAC in Fig. 2.9. As stated in section 2.3, another effective way to improve the dynamic performance is to insert a second array of switches before the final analog output. These backend elements are controlled by the reference clock. Lower glitch energy can be achieved when a fully decoded DAC is used in the DDFS architecture [55]. However, a segmented DAC architecture is typically employed due to a trade-off between the achievable glitch energy and the decoder area. The worst case glitch energy will now depend on the selected segmentation level [60].

3.4.3 Transistor level and SFDR simulation

Transient simulations were carried out in order to evaluate the performance when operating at 3.4GHz (6.8GS/s). The clock signal in Fig. 3.26 contains a random jitter component following a normal distribution with $\mu = 0$ and $\sigma = 3.3$ps (~ 20ps from -3σ to

3σ). Note the correspondence with the behavioral model in Fig. 3.23. The worst case SFDR was obtained at the 3.4GHz clock frequency and F_{OUT} = 2.26GHz (Fig. 3.27) [60]. An ideal Verilog-A model of the 2I-DAC was employed to generate the analog waveform from the two complementary digital outputs of the DDFS (*SINE_ODD* and *SINE_EVEN*). The SFDR performance from DC to Nyquist frequency (3.4GHz) when operating at 6.8GS/s (F_{CLK} = 3.4GHz) is summarized in Fig. 3.28. Simulation results for SS, TT and FF corners were included in order to validate the circuit behavior under manufacturing process variations. The upper bound of the SFDR due to the phase truncation effect was estimated to be 84.28dBc from (3.1). However, the results in Fig. 3.28 show a worst case SFDR of 61dBc. As expected, the selected values for *T*, *P* and *A* lead to an output signal distortion that is mainly determined by the DAC performance.

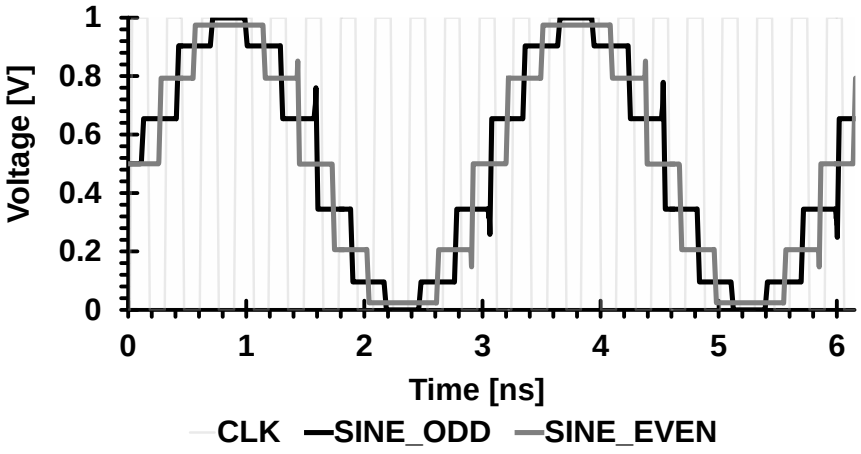


Fig. 3.26. Transient simulation. F_{CLK} = 3.4GHz. F_{OUT} = 340MHz.

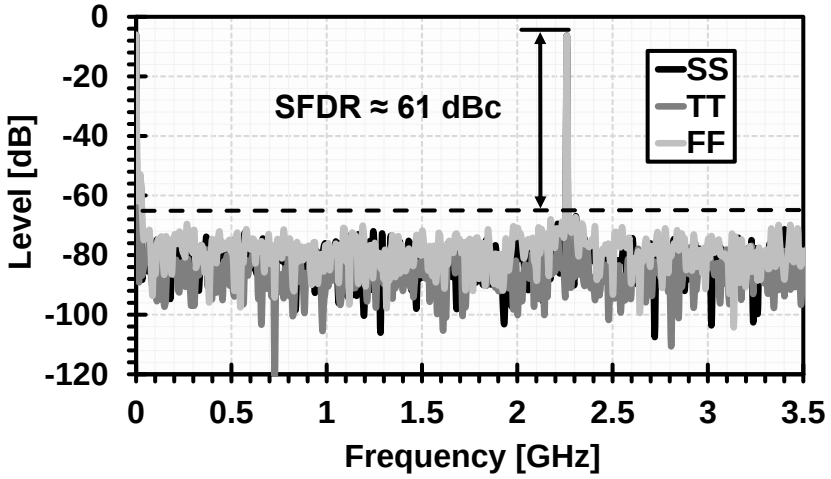


Fig. 3.27. Worst case SFDR. F_{CLK} = 3.4GHz. F_{OUT} = 2.26GHz.

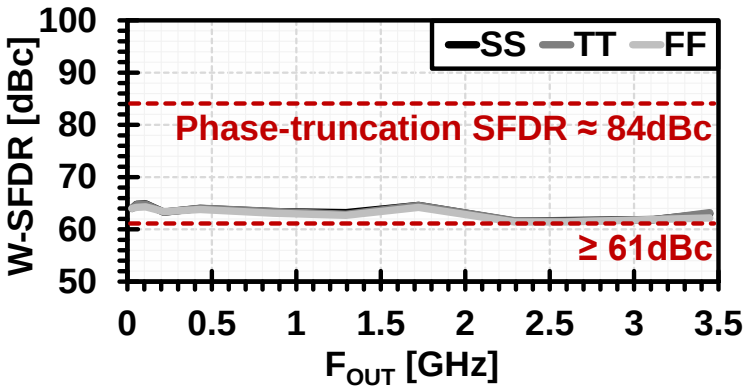


Fig. 3.28. SFDR vs DDFS output frequency. F_{CLK} = 3.4GHz.

The artifacts generated by the phase truncation mechanism in the DDFS are masked by the noise floor of the DAC. In these simulations, the main contributors to SFDR degradation are the aliasing spurs due to the sampling nature of this system and an amplitude quantization noise correlation that depends on the *FCW* value for a given sampling rate. As a consequence of the second mechanism, the spectral content of the quantization noise does not follow anymore the white noise distribution model [56]. In Fig. 3.27 the worst case spur corresponds to the alias component of the second harmonic (2.28GHz) [60].

3.5 Performance comparison

An equivalent NCO using flip-flop as the synchronizing element was designed in order to benchmark the system performance (Table 3-2). The proposed architecture allows for virtually doubling the data sampling rate while trading-off area and power efficiency. In section 6.1, the clock skew that guarantees an error-free operation of the proposed DDFS was found to be 20ps. However, according to the static timing analysis results, the flip-flop-based design listed in Table 3-2 can tolerate a skew of only 8ps when operating at the maximum sampling rate. A clock uncertainty superior to that value can either generate a max-timing or min-timing violation. The period limitation imposed by the strict timing constraints in the flip-flop-based topologies, not only prevents to borrow time between successive pipeline stages, but also imposes more strict constraints on the clock source and distribution network. As a result, the maximum operation speed is limited to 3.5GS/s by the DDFS internal logic regardless the performance of the selected DAC. Although a second DDFS core can be used in parallel to duplicate the operation speed of the system, the active area will be increased (0.11mm^2) when compared with the proposed design (0.079mm^2) [60].

TABLE 3-2: PERFORMANCE BENCHMARK.

	This Work	Reference design
Architecture	DM	
	Pipelined PA	
	SoP terms-quarter wave symmetry based PAC	
	Complementary dual-phase latch-based	Flip-flop-based
T	24	
P	14	
A	10	
CMOS technology [nm]	65	
Sampling rate [GS/s]	**6.8**	3.5
Active area [mm^2]	0.079	0.055
PE [mW/(GS/s)]	22	54

3.6 Summary of the complementary dual-phase latch-based NCO

In this chapter, a 24-bits complementary dual-phase latch-based phase accumulator and a dual-phase sum of product terms based phase to amplitude converter are presented. These two solutions compose the introduced high-speed NCO circuit. The combination of the proposed techniques results in a complementary and parallel architecture that can output two samples per clock cycle and achieve a 6.8GS/s operation in 65nm CMOS technology by simulation. Compared to conventional NCOs using flip-flops as the synchronizing elements, the proposed architecture allows for virtually doubling the data sampling rate while trading-off area and power efficiency. The occupied active area is only 0.079mm^2. A maximum data sampling rate of 6.8GS/s and a power efficiency of 22mW/(GS/s) is expected. An improvement in the total power consumption was achieved when compared with the combined contributions from the C2P-PAC and SoP-PAC blocks (sections 3.1 and 3.2). The enhanced performance results from the sharing and optimization of a common clock tree network. This system can tolerate up to 20ps clock skew without loss of performance when operating at maximum frequency. The worst case simulated SFDR is 61dBc; however, the dynamic performance will be mainly determined by the integrated DAC. This architecture can be used in combination with two parallel DAC cores operating alternatingly (2I-DAC).

CHAPTER 4:
TWO-TIMES INTERLEAVED RDAC

THE proposed NCO architecture features a complementary pair of digital outputs (*SINE_ODD* and *SINE_EVEN*) and is suitable for driving an interleaved-DAC. In this type of converters, two sub-DACs are synchronized with opposite phases of the clock and share a common output node. Conventional interleaved DACs are implemented by using current-source based cells and suffer from code-dependent output impedance and a signal swing limited by the available voltage headroom [64]. The advantage of the current-source cell resides in the fact that the PVT variations can be compensated by adjusting the bias voltage. On the contrary, the value of the ohmic element in a resistor-based cell is fixed [64]. DEM methods can be employed in this second alternative to compensate the distortions due to PVT variations. The resistor-based cells have wider output swing, code-independent output resistance, and better substrate noise immunity (unsilicided P+ polysilicon resistors are commonly used) [64]. A detailed view of the proposed converter architecture based on resistor-based cells is depicted in Fig. 4.1. The DSP engine includes an array of RETIMING flip-flops before segmenting the data into a 4-bits LSB binary section and a 6-bits MSB unary section. The RSTC-DEM method was used in order to reduce the non-linear effects due to resistor mismatches [55]. A DELAY BALANCE structure aligns the binary data with the randomized outputs from the RSTC-DEM core. A code-dependent switching stage (S_{ODD}/S_{EVEN}) connects the differential resistive array (RDAC_A-RDAC_B) either to V_{DD} (1.2V) or V_{SS}. The access to the V_{OUTP} and V_{OUTN} outputs is arbitrated by a row of interleaving switches enabled by the F_{DAC} clock. In this way, the distortion resulting from the code dependent glitches can be diminished [54]. The binary section is implemented as a voltage-mode R-2R ladder network. An additional RDAC cell is needed because the THERMOMETER coded outputs are extended to 64-bits. One of these cells is randomly disabled (dummy) according to the RSTC-DEM sequence. As a result, the RDAC operation becomes equivalent to a conventional one but with an arbitrarily selected resistor bank (63 (RDAC_A) + 63 (RDAC_B) unary cells are simultaneously enabled). A hybrid clock distribution

network was used in order to minimize the systematic skew as well as the random and drift distortions due to on-chip variations (OCV) [65]. However, this architecture draws a code dependent current from the power supply, this can be also understood as a code dependent input impedance (Fig. 4.2) [65]. The maximum bonding wire length in the employed low profile quad flat package (LQFP) is 3.7mm. With an inductance and resistance that can be roughly approximated to 1nH/mm and 0.1Ω/mm respectively [66], 3.7nH and 0.37Ω interconnection parasitics are expected.

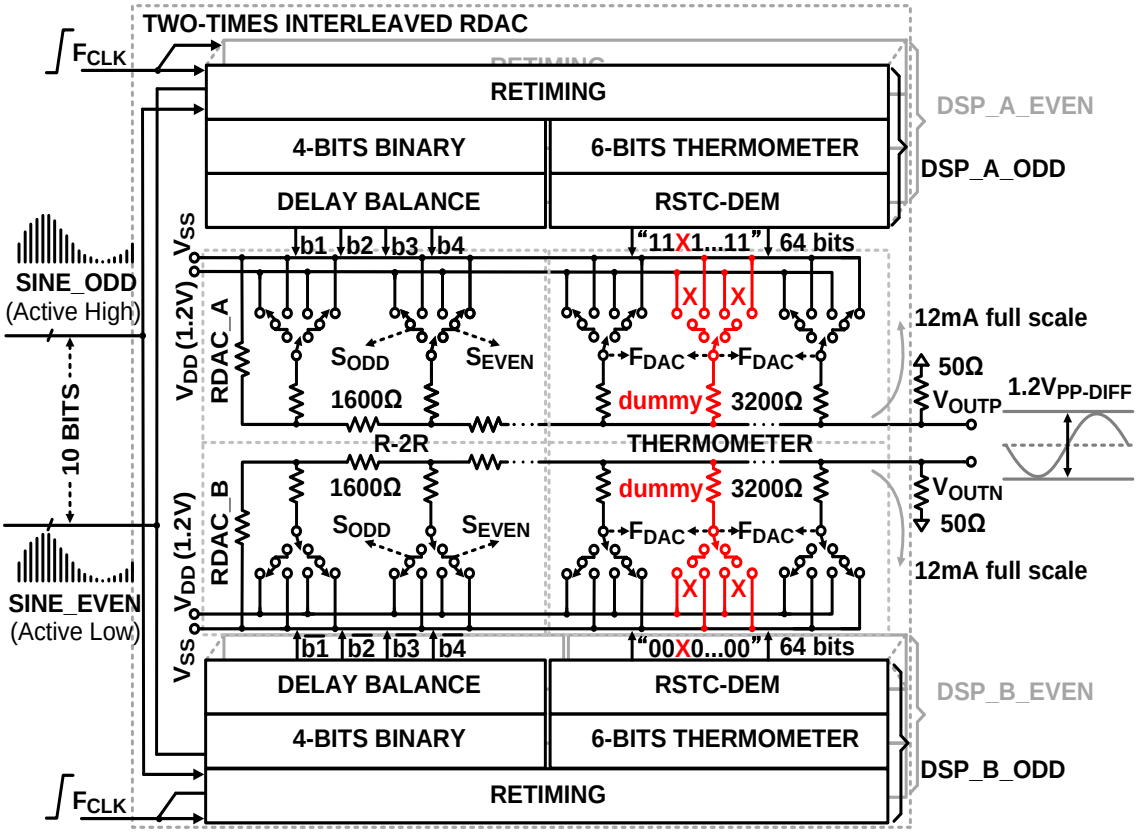


Fig. 4.1. Two-times interleaved RDAC architecture.

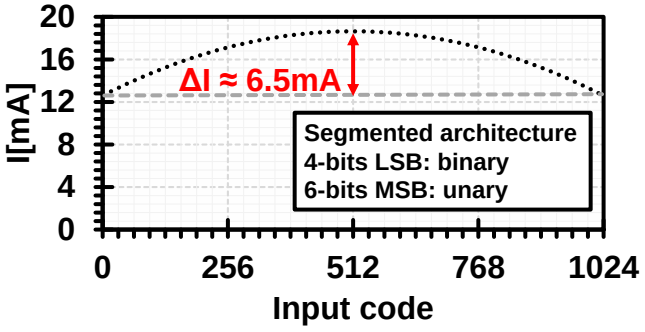


Fig. 4.2. Code dependent current drawn from the power supply.

These non-idealities in the power rails, combined with the code dependent current drawn from the power supply, will create a non-linear distortion that results in undesired spectral lines. In order to minimize these effects, the reference voltage input must be driven from a very low impedance power supply. Low impedance traces are also required in the on-chip power distribution network. Since the last interleaving stage is controlled by the clock signal, the skew balance also becomes critical [65].

4.1 High-speed architecture for random swapping thermometer coding dynamic element matching

The RSTC-DEM method proposed in [55] is capable of suppressing the distortions caused by the device mismatches while keeping the glitch energy at the levels of a thermometer coded converter. This architecture resembles the block diagram depicted in Fig. 4.3. The throughput can be increased by using extended versions of a thermometer and 1-hot encoders (‘0’&THERMO and ‘0’&1-HOT) that are also embedded in a mixed-signal topology with reduced combinational latency in the feedback paths [65]. The conventional *N*-bits RSTC encoder comprises a binary-to-thermometer encoder (THERMO), a barrel rotator (ROTATOR), and other control logic. The rotator is employed to shift the starting element of the thermometer code generated from the binary values *x(n)*. A multiplexer/demultiplexer pair (DEMUX/MUX), two registers (A and B), and an adder/subtractor (ADD/SUB) unit compose the circuit implementing the random swapping operations. A 1-bit random sequence (*R*) indicates the selecting direction and is generated from a pseudorandom binary sequence generator (PRBS). The input signal and the control index of the barrel rotator are synchronized by using flip-flops (FF) to ensure a proper timing [55].

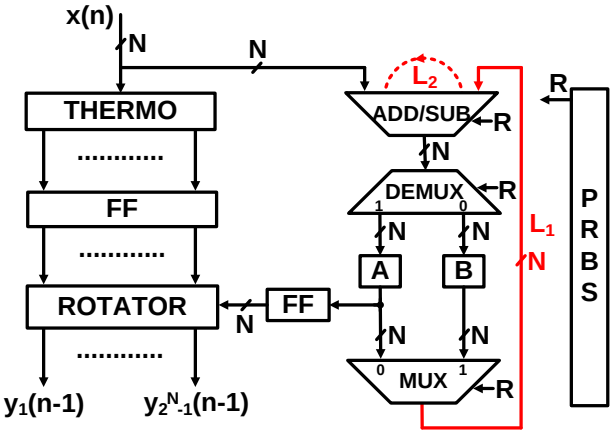


Fig. 4.3. Conventional *N*-bit RSTC-DEM encoder.

The simulation results in [55] indicate that this algorithm can effectively improve the SFDR by randomly changing the selecting direction of the unary coded signals driving the DAC cells. However, up to date, the application of this method has been limited to low-speed systems (≤ 200MS/s) [58]. This recursive system restricts the use of pipelining and parallel structures during the timing optimization process. The main limitations reside in the digital feedback-loop structures employed in the RSTC encoder. A first loop (L_1 in Fig. 4.3) is used in order to feedback the values from either register, *A* or *B,* for the next cycle operations in the ADD/SUB block. A second loop (L_2 in Fig. 4.3) is needed in order to implement the modulo 2^N-1 operation required by this algorithm. Note that the valid numbers in the architecture proposed in [55] range from 0 to 2^N-2. The value 2^N-1 is forbidden because the bit positions in the thermometer coded signals range from 0 to 2^N-2 (2^N-1 bits), creating the need for a condition-detector loop inside the arithmetic unit (ADD/SUB). These two loops difficult the use of pipelining and parallel structures in order to speed up the system performance. Hence, limiting the maximum sampling rate of the system [67]. An architecture with reduced delays in the feedback loops is proposed in this dissertation (Fig. 4.4).

A dummy "0" is inserted in the MSB position of both the '0'&THERMO and '0'&1-HOT generated codes. As a result, a high-speed and low-complexity modulo 2^N addition-subtraction unit (ASU) based on a pipelined ripple-carry adder-subtractor topology can be employed (the modulo 2^N-1 operation in [55] is no longer required). The ASU_ODD and ASU_EVEN signals drive the modified one-hot code ('0'&1-HOT) and ROTATOR blocks in Fig. 4.4. A feed-forward section comprising the '0'&1-HOT encoder and an ARBITER circuit was adapted to the original structure in [55]. The combinational delay in the parallel loops (L_3-L_6 in Fig. 4.4) is now only constrained by the ASU internal logic. A complementary dual-phase latch-based '0'&THERMO encoder was designed in order to match the NCO core timing performance. This block was made up of AND/OR gates inserted into 5 pipeline stages (P_1 to P_5 in Fig. 4.5 a)). Similarly to the PAC design, this block is made up of combinational logic. The thermometric signals are implemented in the form of SoP terms obtained from a 6×64 bits binary-to-thermometer lookup table (including one extra dummy "0" in the MSB position). As a result, the proposed encoder can achieve the required sampling rate by using both levels of the clock and exploiting the time borrowing property. The extended one-hot encoder was implemented following the same design methodology adopted for the binary-to-thermometer decoder (Fig. 4.5 b)) [65].

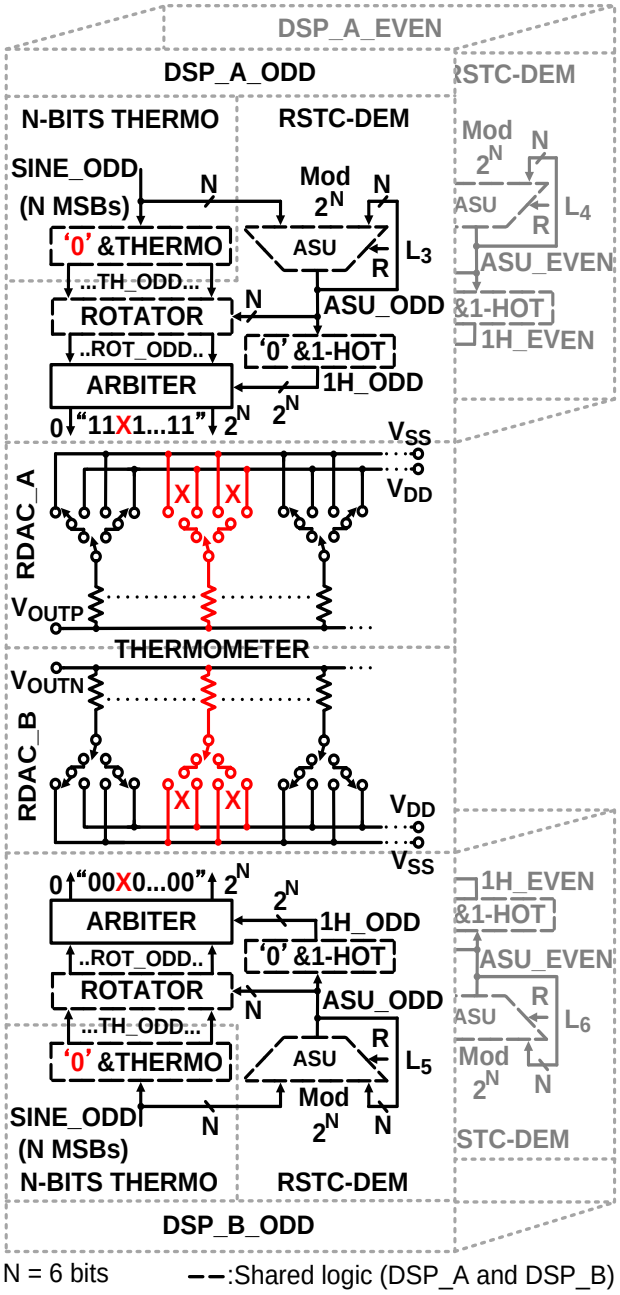


Fig. 4.4. Proposed *N*-bit high-speed RSTC-DEM encoder.

This '0'&1-HOT encoder will always tag the position of the dummy '0' in the randomly shifted thermometer coded sequence. This core was also synthesized from a 6×64 bits binary-to-one-hot lookup table (including an extra dummy '0'). The extended-one-hot encoder requires two stages of AND/NOT gates to perform the tracking operations. The barrel ROTATOR was implemented by using a conventional multiplexer-based architecture divided into 6 complementary dual-phase latch-based pipeline stages. It randomly swaps the elements in the extended-thermometer coded

sequence while the '0'&1-HOT unit tags the position of the dummy '0' [65]. For simplicity purposes, only the ASU block corresponding to the $SINE_{\_ODD<4>}$ and $SINE_{\_EVEN<4>}$ signals is represented in Fig. 4.6.

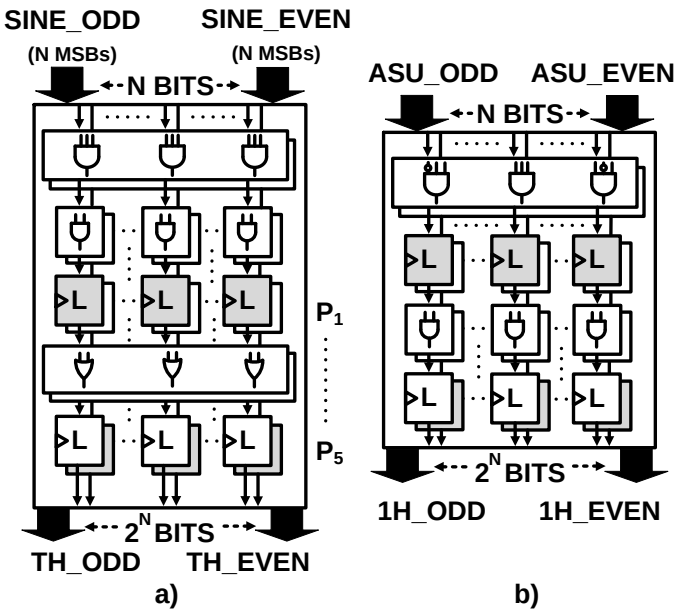


Fig. 4.5. High-speed encoders. a) Binary-to-thermometer. b) one-hot encoders.

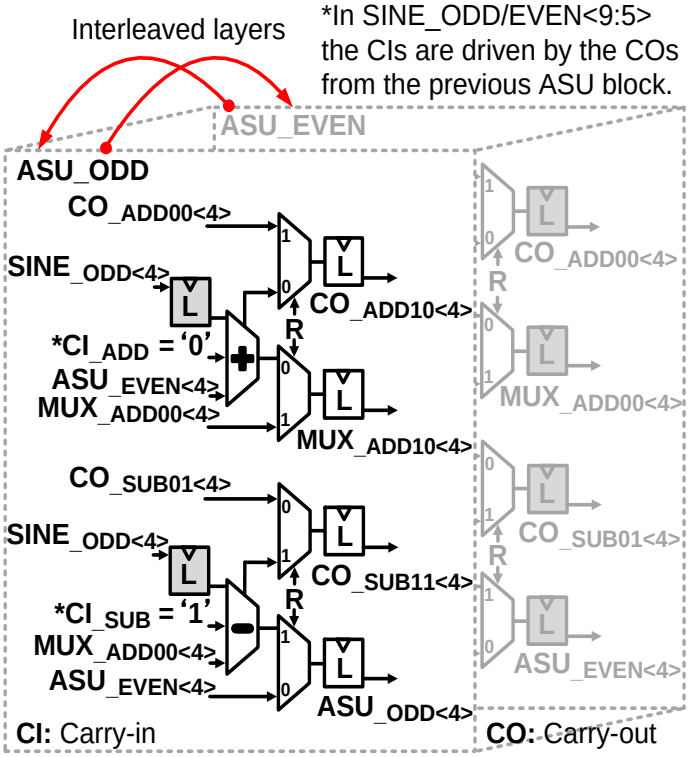


Fig. 4.6. Complementary dual-phase latch-based ASU.

Each complementary layer (ASU_ODD and ASU_EVEN) includes a 1-bit full-adder, a 1-bit subtractor, multiplexers, and latch cells. The postfixes $_X$ and $_Y$ in the $CO\_ADDXY<4>$, $CO\_SUBXY<4>$, and $MUX\_ADDXY<4>$ signals respectively represent the active levels of the clock and an on-chip generated pseudorandom binary sequence (R). Depending on the logic values at R during the active level of the clock (F_{LOGIC}) a new arithmetic operation is multiplexed or the previously calculated values are retained. In this way, the random swapping operations described in [55] can be executed. The algorithm introduced in [55] requires that the $CO\_ADD10<4>$ and the $MUX\_ADD10<4>$ signals in the ASU_ODD block takes the values from the ASU_EVEN module outputs if $R = 1$ and the F_{LOGIC} is at the "high level". Conversely, this signals will be updated with a new addition result if $R = 0$ and $F_{LOGIC} = 1$. Equivalent operations are executed in the ASU_EVEN block by multiplexing the previous data from the ASU_ODD unit or the new arithmetic results calculated from the pipelined $SINE\_EVEN<4>$ (always when F_{LOGIC} is at the "low level"). Similarly, the $CO\_SUB11<4>$ and the $ASU\_ODD<4>$ signals update its current value from the ASU_EVEN module outputs if $R = 0$ and F_{LOGIC} is at the "high level". A new subtraction operation is executed if $R = 1$ and $F_{LOGIC} = 1$. The $CO\_SUB01<4>$ and the $ASU\_EVEN<4>$ signals are updated with a new subtraction value when $R = 1$ and $F_{LOGIC} = 0$. Otherwise, when $R = 0$ and F_{LOGIC} is at the "low level', previous values from the complementary ASU block are multiplexed. Note that, depending on the R value, the $ASU\_ODD<4>$ and $ASU\_EVEN<4>$ signals keep the previous values from the complementary block or take those from the current subtraction unit. Likewise, the carry outputs $CO\_ADDXY<4>$ (addition) and $CO\_SUBXY<4>$ (subtraction) will be always updated according to the previous or current equivalent operation. The diagram in Fig. 4.6 can be extended to an N-bits arithmetic unit by inserting N concatenated ASU blocks into an array of pre/post-skewing latches. A 6 bits addition-subtraction module was employed in this work. The resulting data sequence in the ASU_ODD and ASU_EVEN signals is equivalent to the one stored in the register A in Fig. 4.3, but consecutively updated during both levels of the clock. In this way, the proposed unit can execute the RSTC-DEM mechanism [55] but with a worst case combinational delay of only 1-bit adder/subtractor plus one multiplexer cell in the feedback-loops (L_3, L_4, L_5 and L_6 in Fig. 4.4). Because complementary latches are used as synchronizing elements, the encoder can operate during both high and low levels of the clock. The time borrowing property can be also exploited in order to equal the throughput of the NCO core [65].

The ARBITER circuit will drive the SW_N_O and SW_P_O (or SW_N_E and SW_P_E) signals (Fig. 4.7) in a way that both pass-gate switches (PG) in the dummy

cell are OFF, making N_1 (or N_3) a high-impedance node. Although this interruption will generate some disturbance in the circuit, it follows a random disconnection pattern and will not have a major impact on the SFDR performance. This functionality is implemented in the ARBITER circuit as an array of OR, XOR, and NOT gates (Fig. 4.8). The ARBITER block also generates the non-inverted (RDAC_A) and inverted (RDAC_B) values required by the differential architecture. These signals follow the sine waveform information generated in the PAC block and drive the first switching stage in the RDAC cells. The data needs to be aligned by using flip-flops after being retimed during the time borrowing process in the DSP units [65].

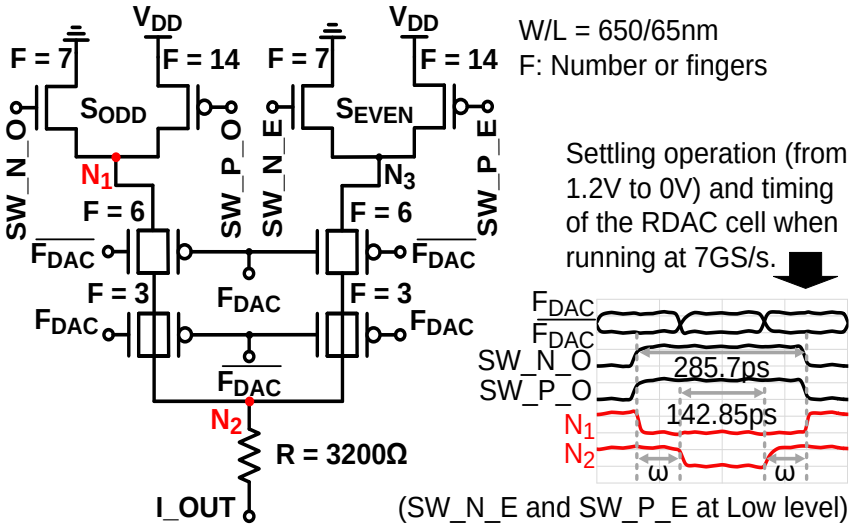


Fig. 4.7. RDAC cell.

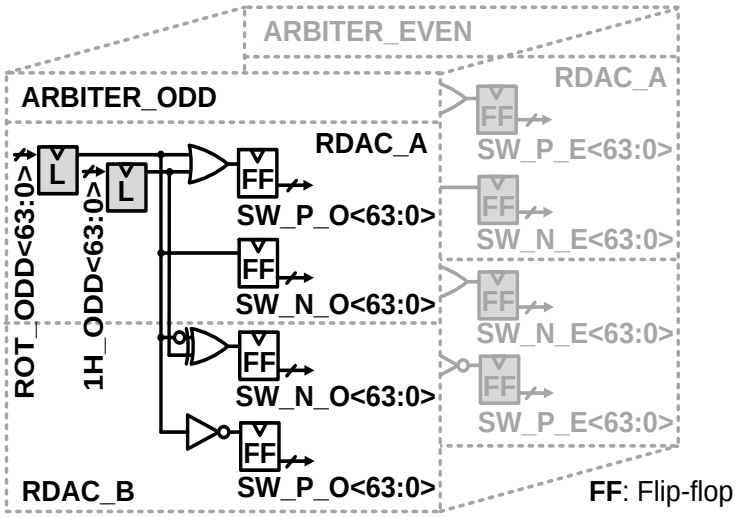


Fig. 4.8. ARBITER circuit.

4.2 RDAC cell

The RDAC cell in Fig. 4.7 is a simple circuit that can occupy a relatively small footprint. As can be noticed from the timing diagram also in Fig. 4.7, when the control signals at the gates of the code-dependent stage (*SW_N_O* and *SW_P_O*) are toggled to V_{DD}, the N_1 node is connected to ground potential. However, the N_2 node does not take the new voltage value until the transmission-gate (TG) in the interleaving stage is turned ON. Therefore, the distortion resulting from the code-dependent switching activity can be reduced by disconnecting the output node during the transition of the data dependent switches. This can also relax the settling time and slope requirements of the data control signals. This cell includes a two-times interleaved switching stage controlled by the reference clock (F_{DAC}) and implemented by using transmission-gates. A pair of dummy TGs with half the size of those in the interleaving structure is used to provide additional charge injection and clock feedthrough suppression. These dummy switches are driven by the complementary phase of the clock controlling the second interleaving stage. Although by using TG based switches the charge injection and clock-feedthrough effects can be diminished (the complementary signals will act to cancel each other) [64], a residual distortion can still be present in the output due to imperfect matching of the transistors and switching time of the complementary control signals. A dummy pair of TGs with half the size of those in the second interleaving stage are used in order to provide additional suppression [68]. Since the last interleaving stage is controlled by the F_{DAC} signal, the clock skew balance becomes critical in this architecture. The data period is equal to 285.7ps when operating at 7GS/s. Under this condition, the clock half-period is equal to 142.85ps (50% duty-cycle), and a time margin window (ω) of 71.425ps is obtained (Fig. 4.7). A precise control of the clock skew is required in order to guarantee an output transition when the reference data switches were already toggled and the voltage level in N_1 is stable. Also, an accurate balance of the switching and crossing point of the complementary clock signals at the TG gates is required [64]. This structure is sensitive to clock skew and duty cycle variations and requires careful driver design and timing balance [65].

4.3 Hybrid clock distribution network

A hybrid clock distribution network was used in order to reduce the OCV associated distortions while keeping a reasonable power dissipation and routing congestion metrics (Fig. 4.9). The distribution network is segmented into a clock-tree section, a local-mesh and an array of pseudo-differential drivers. A duty cycle of about

50% was obtained in F_{CLK} after dividing by two an off-chip reference clock independently of its pulse width. The proposed DSP units can tolerate a certain amount of clock skew without loss of performance because the complementary dual-phase latch-based sequencing method was employed.

Furthermore, the maximum amount of clock skew that can be tolerated will increase proportionally with a decrease in the clock frequency. Correspondingly, for a fixed borrowed time, the system clock skew tolerance will also increase. For these reasons, a simple clock-tree structure can satisfy the timing requirements of the digital sections. However, a precise control of the clock skew is required in the RDAC cells [65]. A clock-mesh driven by a global network containing 3 levels of sub-trees is employed in this case. Compared to a simple clock-tree, this hybrid approach is less affected by the skew due to non-uniform load distribution. The local-mesh section also compensates much of the random skew by shorting together the clock buffer outputs [52]. Finally, a pseudo-differential driver is used in order to locally distribute the $F_{DAC}/\overline{F_{DAC}}$ clocks and balance its duty cycle [69]. This structure is composed of two buffered stages containing cross-coupled inverter pairs (Fig. 4.9). The selected inverter sizes can provide a 20ps slew-rate when loaded with the TGs in the RDAC cells. Table 4-1 shows the timing error between the interleaved channels resulting from duty cycle distortions (transistor level simulations at different PVT corners). It should be noticed that, whit a 3.5GHz clock, the sampling error in the N_2 node (Fig. 4.7) is about 3ps in the TT/1.2V/25°C corner. Under these conditions, a worst case W-SFDR around 30dBc is expected (Fig. 2.7) [65].

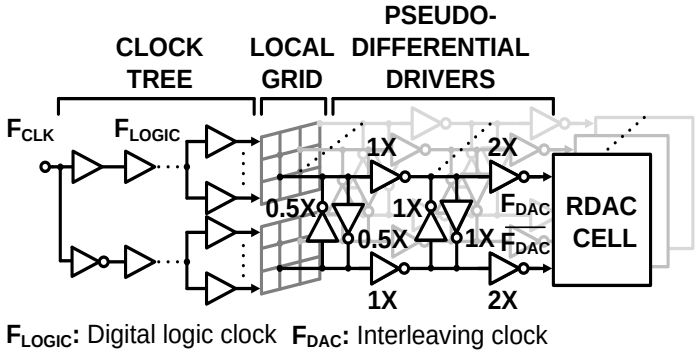


Fig. 4.9. Hybrid clock distribution network.

TABLE 4-1: SAMPLING ERRORS CAUSED BY DUTY CYCLE DISTORTIONS

Corner	0.9V/75°C	1.2V/25°C			1.2V/-25°C
	SS	FS	TT	SF	FF
Sampling error (N_2, Fig. 4.7) [ps]	10.8	6.3	3.3	1.7	1.9

The combination of dual-phase latch-based DSP units with a hybrid clock distribution network can increase the tolerance to OCV compared with conventional flip-flop based architectures driven by a pure clock-tree structure. However, the clock-mesh section consumes more routing resources and exhibits a higher switching capacitance and power consumption [52].

4.4 Static timing analysis

Static timing results were obtained by employing Synopsys/Design-Compiler/IC-Compiler/PrimeTime toolset at the TT/1.0V/25°C corner. Behavioral, post-synthesis and back-annotated post-layout simulation were completed with Cadence/NCsim simulator. In all cases, the interconnection parasitic values were derived from a layout parameter extraction (LPE) database including the cross-coupling associated delays. The timing relationships in Table 2-1 characterizes the complementary dual-phase latch-based synchronization method [52]. The presence of clock skew results in a decrease of the maximum available borrowed time. Therefore, the max-timing constraint is unaffected if there is enough time headroom to allocate the clock skew. However, the min-timing constraint is not immune to variations in the edges of the reference signal, making this requirement more stringent as the clock uncertainty worsens [52]. Table 4-2 summarizes the post-layout static timing analysis (STA) results. The multiplexing logic in the ROTATOR constitutes the critical path in terms of max-timing. The worst case min-timing occurs between the back-to-back latches used in the one-hot encoder in order to balance the pipelining length across the RSTC-DEM core. The mixed-signal system was evaluated under different PVT conditions (SS/0.9V/75°C, TT/1.2V/25°C and FF/1.2V/-25°C) by running transistor level simulations with back annotated delay information in Cadence/APS. Although no direct reports about the min-timing and max-timing were obtained, the proper sampling of the digital data in all the simulated corners was verified during the transient simulations. Two main conclusions can be formed based on the STA data reported in Table 4-2.

TABLE 4-2: WORST CASE PATH STA RESULTS (TT/1.0V/25°C CORNER).

Maximum F_{CLK} [GHz]	3.4		
Sampling rate [GS/s]	6.8		
Max-timing		**Min-timing**	
Minimum $T_{c/2}$ [ps]	147	**Libray T_h [ps]**	-27
Libray T_s [ps]	31	**Libray T_{ccq} [ps]**	41
Maximum T_b [ps]	116	**Maximum T_{skew} [ps]**	68
Actual T_b [ps]	81	**T_{min} [ps]**	0
Maximum T_{skew} [ps]	35		

First, in terms of max-timing constraint, the system can tolerate up to 35ps of clock skew when running at 6.8GS/s. A variation in the clock edge transition up to that limit will only increase the actual T_b and will not generate any max-timing violation. When the resulting T_b value (the actual T_b plus the clock skew) equals the maximum T_b (116ps), the system is running without any margin and a further increase in the clock uncertainty will generate timing violations. This point corresponds to a T_{skew} = 35ps. Second, because the hold time (T_h) of the latches in the employed 65nm CMOS library is a negative value (-27ps in the worst-case path), the min-timing constraint is less restrictive. According to static timing analysis results, the maximum clock skew that produces no min-timing violations is 68ps. Under these conditions, the T_{min} is equal to 0s, meaning that even back-to-back latches can be employed without incurring in minimum timing violations. Consequently, the performance of the DSP units is limited by the max-timing constraint. The complete-DDFS-solution composed by the NCO in Chapter 3 and this converter will be limited by the worst case clock skew in the NCO core (20ps), and not by the RDAC digital logic (35ps) [65].

4.5 Mixed-signal layout considerations

In mixed-signal applications, the layout characteristics may have an impact on the final quality of silicon (QoS) metrics. Proper segregation between the analog and digital circuits should be guaranteed by a careful floorplanning. Sensitive analog nodes must be isolated from potential noise sources like digital blocks with fast switching activity. Grounding and power supply should be also separated when using digital and analog circuitry on the same substrate [64]. Analysis including realistic wire delay information must be also performed as they become a critical aspect in high-speed systems. All the digital logic was designed by using standard-cell technology and a fully synthesizable flow including automatic place and route. Design-Compiler topographical mode was employed during the synthesis step. This tool can predict the post-layout delay information by using more realistic interconnection parasitics. Consequently, the correlation between the post-synthesis and post-layout quality of results is improved. A signal integrity analysis was performed during the place and route stages in order to guarantee a low IR drop, electromigration, and crosstalk. A symmetrical layout including dummy elements was employed in order to improve the matching properties among the differential RDAC architecture (Fig. 4.10).

By using separated pins and pads in a triple-well process, the analog and digital power rails were properly isolated. Multiple power supply pins were employed in order

to reduce the distortions associated with the bonding wires parasitics. A common analog voltage supply and ground (V_{DD} and V_{SS} in Fig. 4.10) with symmetrical and low impedance traces were implemented in order to reduce the non-linear distortions due to the variable input impedance. The RDAC complementary outputs (V_{OUTN} and V_{OUTP}) were placed close to the pads and also surrounded by metal blockage areas in order to limit the interference from the rest of the circuit. The clock mesh and the RDAC cells were laid out manually, minimizing the length of the current-carrying paths, and using redundant vias and contacts. The R-2R and THERMOMETER sections were implemented by employing unsilicided P+ polysilicon resistors with a $3.3\times12.43\mu m^2$ area. The distribution network of the digital power supply was also automatically synthesized. Special attention was paid to the IR drop characteristics to prevent a deterioration of the timing performance due to a non-uniform power supply among the standard cells. Fig. 4.11 represents the digital voltage drop across the DSP cores of the 2I-RDAC. It can be noticed how the worst case condition does not exceed 4mV (0.33% of the nominal voltage (1.2V)).

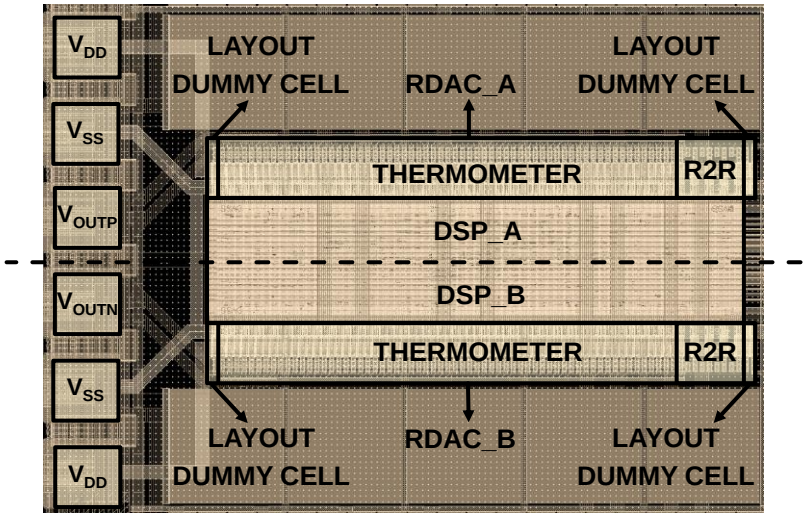


Fig. 4.10. RDAC layout view.

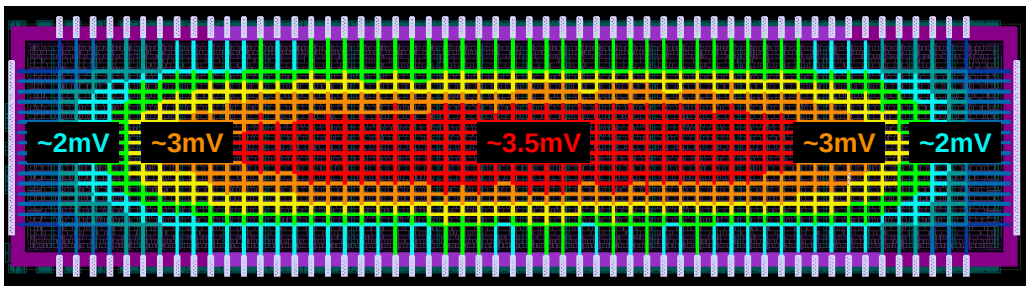


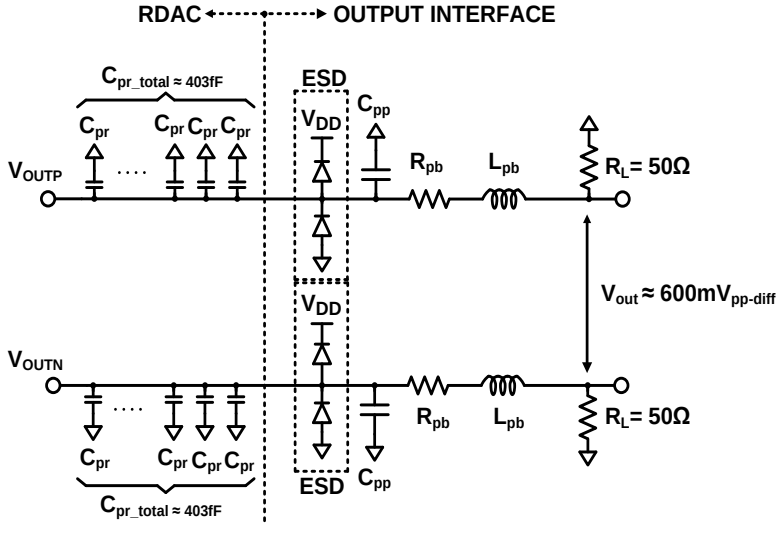
Fig. 4.11. Digital V_{DD}. IR drop in the synthesized power network.

4.6 Design verification

The transistor level simulation was performed with Cadence/APS in order to verify the correct operation of the system when integrating the NCO core described in Chapter 3 and the 2I-RDAC presented in previous sections. These simulations included the parasitic extracted information of critical components such as the clock distribution network, the power supply rails and the output interface. Time and frequency domain simulations were completed in order to evaluate the critical parameters, including the waveform characteristics, SFDR and settling time. All the presented results were obtained at the TT/1.2V/25°C corner.

4.6.1 Settling time

Conventionally, the most important parameter in DDFS applications is the narrowband SFDR (N-SFDR) and the settling time is not commonly reported. However, since an RDAC core is employed, the parasitics in the resistor units and the output pads together with the bonding wire non-idealities, the capacitance of the electrostatic discharge (ESD) protection circuit and the load resistance will limit the realizable throughput. The worst condition occurs when the system operates at the maximum sampling rate while having a full voltage swing at the output node (F_{OUT} = 3.4GHz and SR = 6.8GS/s).



C_{pr}: RDAC unit parasitic capacitante ≈ 6.3fF (3200Ω) (3.3 × 12.43μm²) (LPE)
C_{pp}: Output pad parasitic capacitante ≈ 46fF (62μm × 68μm) (LPE)
R_{pb}: Bonding wire parasitic resistance ≈ 0.37Ω (3.7mm)
L_{pb}: Bonding wire parasitic inductance ≈ 3.7nH (3.7mm)

Fig. 4.12. Output interface simulation model.

The model represented in Fig. 4.12 was used to simulate the transient waveform depicted in Fig. 4.13. It should be noticed that this testbench does not include any noise contribution from the power supply units and assumes a differential 50Ω load after the two off-chip resistors. Under those conditions, a $600mV_{pp\text{-}diff}$ swing is expected. This model also assumes the bonding wires parasitic values as described in Fig. 4.12. According to the LPE models, the selected unsilicided P+ polysilicon resistors (3200Ω) and the output pads (62µm×68µm) have an associated parasitic capacitance of 6.3fF and 46fF respectively. The settling time specification is commonly divided into the slew-time, the recovery-time and the linear-region. As represented in Fig. 4.13, the simulated system has a slew-time of about 105ps (~71.4% of the sampling period at 6.8GS/s). The duration of the recovery zone was recorded up to about 556ps in the same figure. The recovery and linear zones are also magnified in Fig. 4.14. The linear zone lasts for about 160ps until the output settles to within the 1% error band. The obtained settling time was about 820ps by adding the respective contributions of the slew-time, the recovery-time and the linear regions.

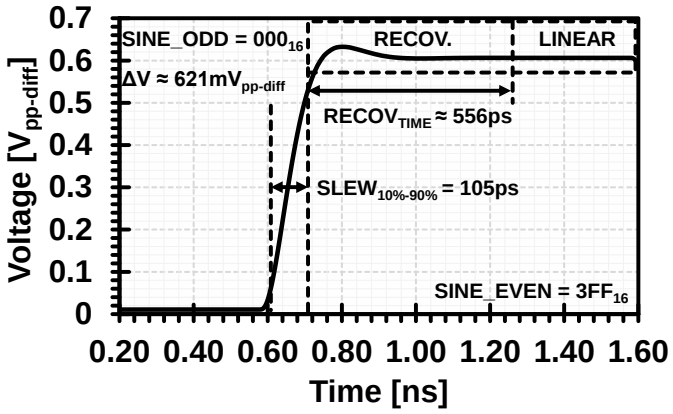


Fig. 4.13. Simulation of the settling time zones.

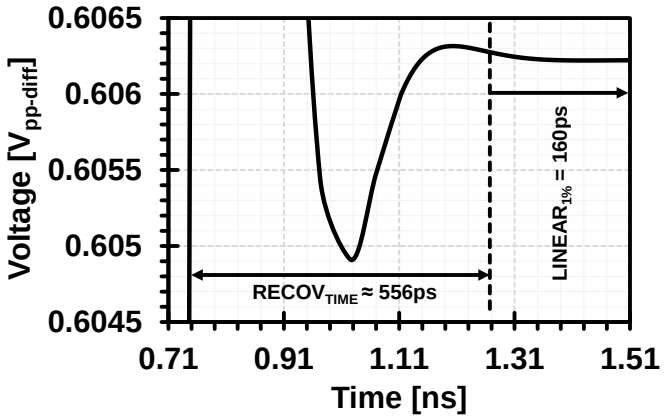


Fig. 4.14. Magnified recovery and linear zones.

4.6.2 Transient simulation

The waveform of an output carrier centered at 299.96MHz is represented in this section. The interface circuit in Fig. 4.12 was also employed in order to evaluate the output waveform characteristics during continuous wave (CW) operation (Fig. 4.15). The V_{OUTP}, $V_{OUTN,}$ and the differential outputs are illustrated. As expected, each signal period is composed on average by 22.6 samples when F_{DAC} = 3.4GHz clock (6.8GS/s).

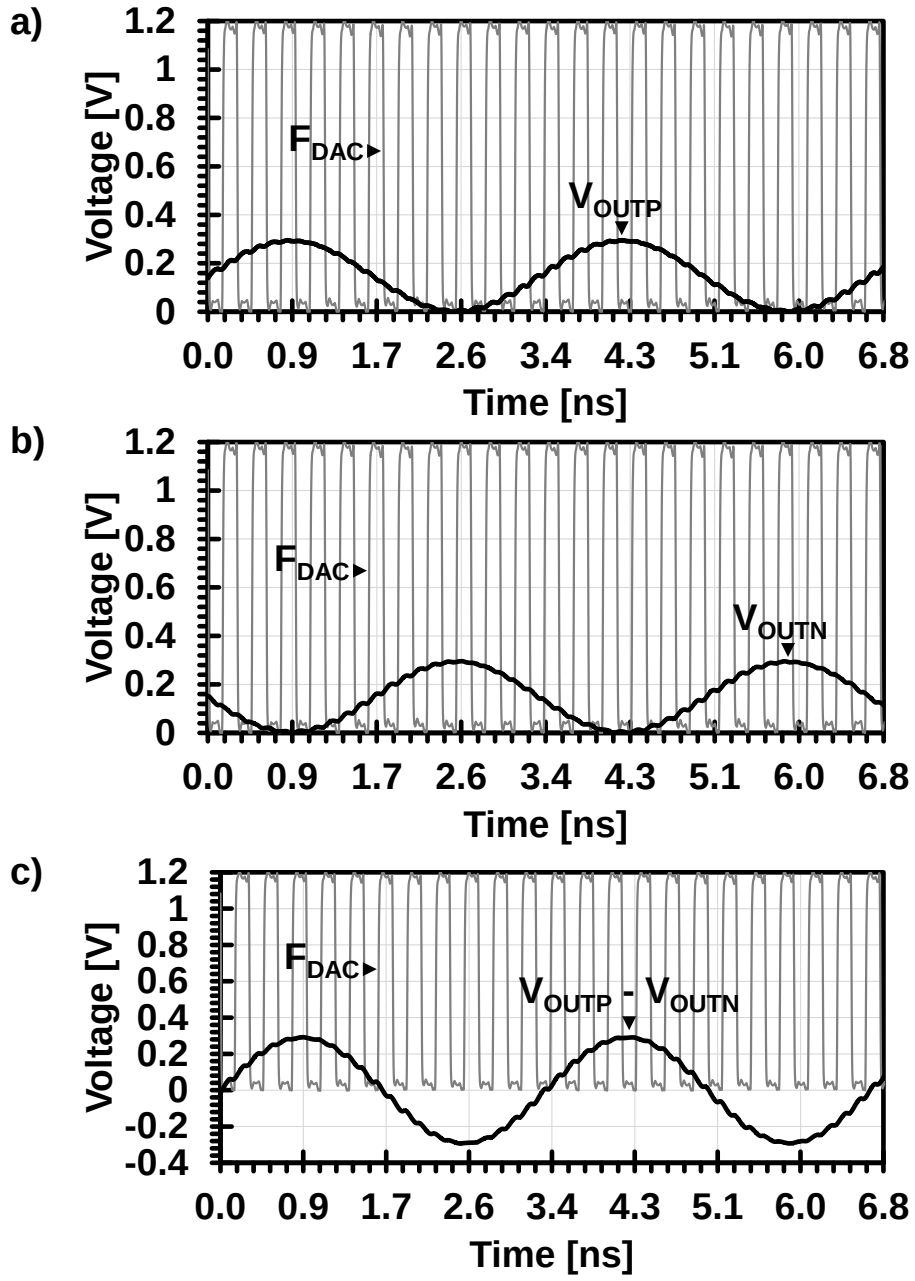


Fig. 4.15. Transistor level simulation. F_{CLK} = 6.8GHz. F_{OUT} = 299.96MHz. a) V_{OUTP} waveform. b) V_{OUTN} waveform. c) Differential output waveform.

The system model also includes the non-idealities in the bonding wires associated with the power supply network and an additive $3mV_{p-p}$ ripple noise. The clock source contains a 700fs RMS jitter component. A resistor mismatch having a normal distribution with μ = 3200 σ = 4.736 (0.148 %) was also adopted (Fig. 4.16).

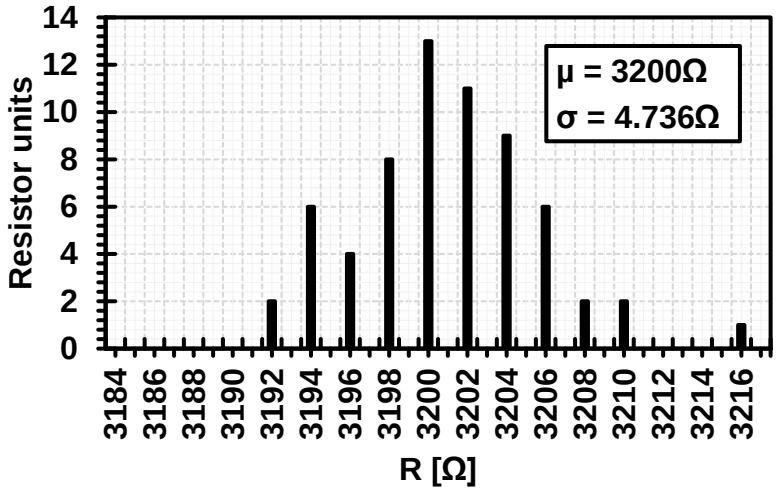


Fig. 4.16. Resistor mismatch model.

4.6.3 Frequency domain

The frequency domain characteristics were simulated at lower synthesized frequencies (F_{OUT} = 299.96MHz) and at higher synthesized frequencies (F_{OUT} = 2.7GHz) whit the RSTC-DEM core enabled and disabled. It can be observed how the interleaving distortions (ID) were dominant in Fig. 4.17 and Fig. 4.18. As expected, the relative level of the interleaving artifact increases in Fig. 4.18 when compared with Fig. 4.17 (section 2.3). The W-SFDR performance from DC to Nyquist frequency (3.4GHz) when operating at 6.8GS/s (F_{CLK} = 3.4GHz) is summarized in Fig. 4.19. Under this conditions, the employed model exhibits a W-SFDR curve that reasonably follows the 3ps timing error profile described in section 2.3.

The W-SFDR at $F_{OUT} \leq$ 299.96MHz was dominated by the third harmonic distortions (3HD). The ID spurs become dominant above that frequency. The second harmonic distortions were sufficiently suppressed by the employed differential architecture to not become determinant in any of the simulated frequencies. It should be also noticed that an increase in the noise floor was observed when enabling the RSTC-DEM (Fig. 4.17 and Fig. 4.18). This is a direct result of the randomization effect over the mismatch errors in the resistor values (Fig. 4.16). No significant improvement in the W-SFDR was registered when enabling the RSTC-DEM core in this simulations.

This can be understood because the effect of the RSTC-DEM is masked by the dynamic errors (harmonics and interleaving spurs) when running at higher sampling rates. However, this method can potentially enhance the N-SFDR by decorrelating the quantization noise in the SoP-PAC and the 2I-RDAC. Due to the multiple variables involved in this process and its different nature (*FCW*, phase-truncation error in the PA, quantization errors in the PAC, conversion errors in the DAC) this hypothesis was confirmed by measurements results in Chapter 6.

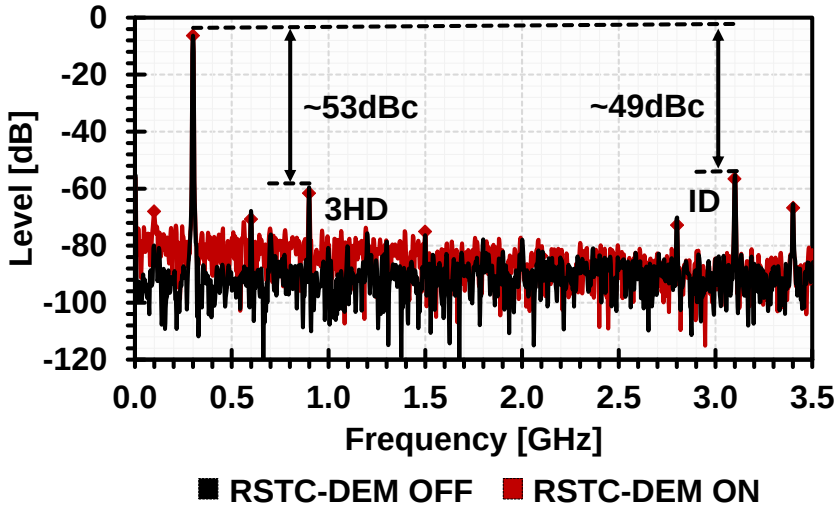


Fig. 4.17. W-SFDR. F_{CLK} = 3.4GHz. F_{OUT} = 299.96MHz.

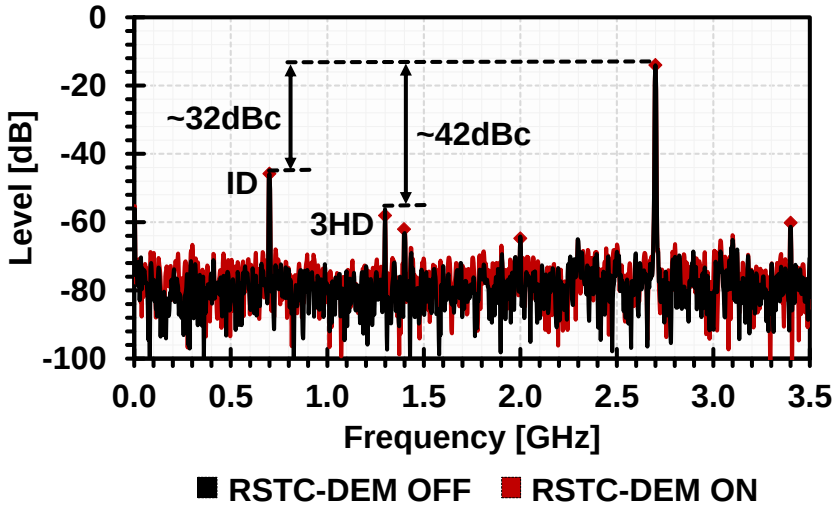


Fig. 4.18. W-SFDR. F_{CLK} = 3.4GHz. F_{OUT} = 2.699GHz.

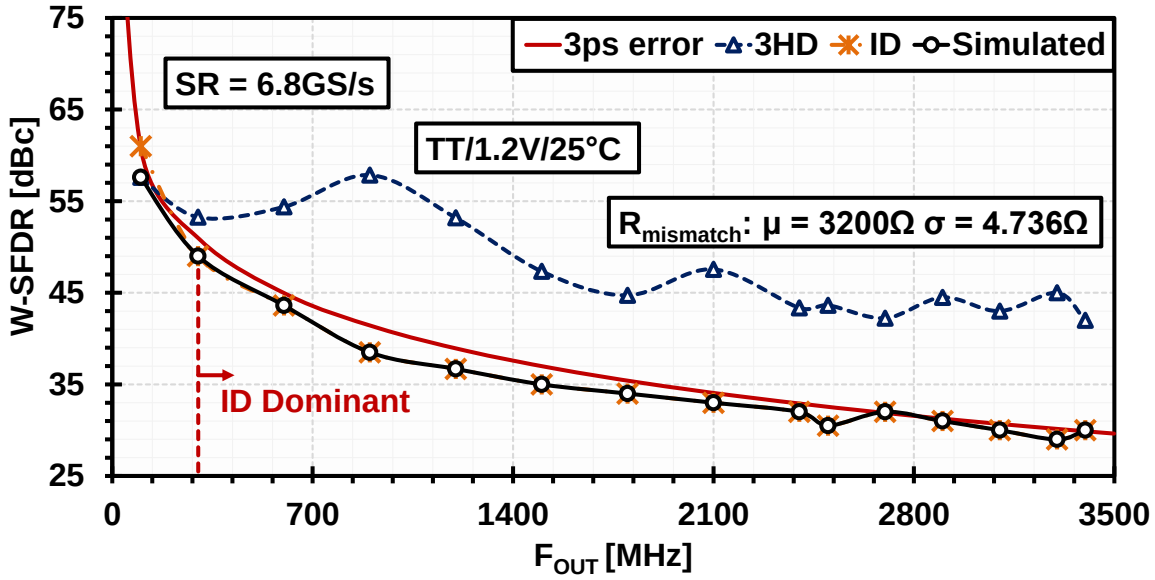


Fig. 4.19. W-SFDR vs DDFS output frequency. F_{CLK} = 3.4GHz.

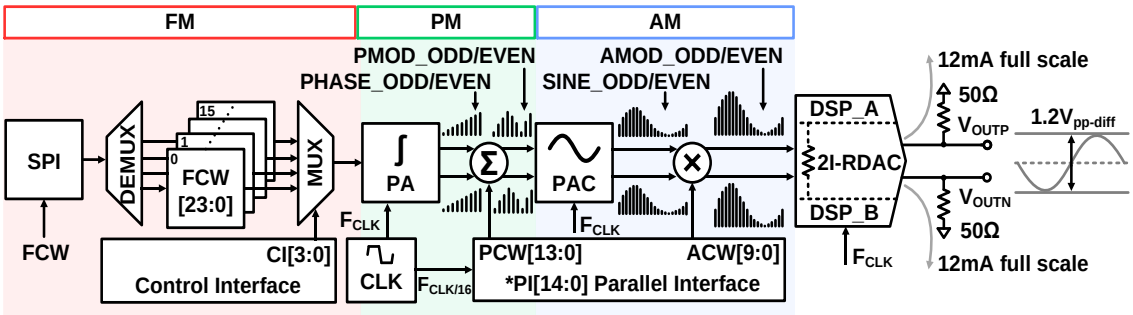
4.7 Summary of the two-times interleaved RDAC

In this chapter a two-times interleaved RDAC unit capable of operating at 6.8G/s in 65nm CMOS technology has been described. Its main advantages are ① a code independent output impedance, ② a rail-to-rail operation can be achieved even under the limited voltage headroom conditions and, finally, by sharing in time a common resistor array among the interleaved digital logic, ③ the system becomes more robust against the inter-DAC gain and offset effects. All the digital blocks were implemented by using a fully synthesizable flow with automatic place and route. A high-speed RSTC-DEM architecture has been also introduced. The analog sections were limited to simple RDAC cells that can decrease the distortion resulting from the code-dependent switching activity by disconnecting the output node during the transition of the data dependent switches. The combination of dual-phase latch-based DSP units with a hybrid clock distribution network can increase the tolerance to OCV compared with conventional flip-flop based architectures driven by a pure clock-tree structure. The simulated sampling error in the output node of the RDAC cells is about 3ps in the TT/1.2V/25°C corner when integrating this converter with the NCO core introduced in Chapter 3. Under this conditions, the employed model exhibits a W-SFDR curve that reasonably follows the 3ps timing error model described in section 2.3 (Fig. 4.19). The simulated results match the expected W-SFDR performance (Fig. 4.19).

CHAPTER 5:

SOLUTIONS FOR HIGH-SPEED DIGITAL MODULATIONS

In order to implement frequency, phase and amplitude modulations in the digital domain, several structures need to be adapted to the high-speed NCO core described in Chapter 3. The required blocks are inserted in the DDFS data path and, as a result, need to run at the same sampling rate of the C2P-PA and SoP-PAC blocks. First, a register bank composed of 16 reconfigurable *FCW* profiles was embedded in the logic. The active *FCW* can be selected among 16 pre-stored values by means of a 4-bits CMOS control interface (CI[3:0]). This conventional topology allows switching the output signal frequency without incurring any extra delay due to the loading sequence of the serial peripheral interface (SPI). Second, a high-speed 14-bits adder and a 10-bits multiplier are employed to perform the phase and amplitude modulation respectively. The complementary dual-phase latch-based sequencing method described in Chapter 2 was also applied in order to speed up the performance of all the digital structures. The system comprises a serial interface and a 15-bits CMOS parallel interface (PI[14:0]) as the input ports for the frequency control word, the phase control word (*PCW*) and the amplitude control word (*ACW*). The general block diagram including the high-speed modulation structures and input interfaces is depicted in Fig. 5.1.



*PI[14] = 0 → PI[13:0] = PCW, PI[14] = 1 → PI[9:0] = ACW

Fig. 5.1. Complete-DDFS-solution architecture featuring FM, PM and AM modulations in the digital domain.

The default data stored in 16 reconfigurable *FCW* profiles are listed in Table 5-1. These frequencies correspond to non-coherent values and cover the first Nyquist zone. The different *FCW*s can be selected via the CI[3:0] interface in order to switch the DM-DDFS output frequency almost instantaneously. Also, the register data can be updated by using the SPI port. Four bits indicating the register address are transmitted in the header followed by a sequence of bits containing the *FCW* to be stored. The frequency tuning resolution (F_{min}) can be calculated from (5.1). Since the selected *FCW* length is 24 bits, the F_{min} becomes 405.3Hz when running at 6.8GS/s.

TABLE 5-1: 16 FCW PRE-STORED VALUES

REGISTER	FCW	FOUT [MHz] @ 6.8GS/s
FCW0	000900_{16}	0.933837891
FCW1	$03C300_{16}$	99.9206543
FCW2	$0B4B00_{16}$	299.9694824
FCW3	169700_{16}	600.0427246
FCW4	$21E100_{16}$	899.9084473
FCW5	$2D2D00_{16}$	1199.981689
FCW6	387900_{16}	1500.054932
FCW7	$43C300_{16}$	1799.920654
FCW8	$4F0F00_{16}$	2099.993896
FCW9	$5A5B00_{16}$	2400.067139
FCW10	$5E1F00_{16}$	2500.091553
FCW11	$65A500_{16}$	2699.932861
FCW12	$6D2D00_{16}$	2899.981689
FCW13	$74B500_{16}$	3100.030518
FCW14	$7C3D00_{16}$	3300.079346
FCW15	$7FF700_{16}$	3399.066162

$$F_{\min} = \frac{SR}{2^{T}} = \frac{F_{CLK}}{2^{T\text{-}1}} = \frac{F_{CLK}}{2^{24\text{-}1}} \tag{5.1}$$

5.1 High-speed phase-adder

A complementary dual-phase latch-based architecture similar to the one employed in the PA design (NCO core) can be adopted in the phase-adder. This unit will take the *PCW* information from the parallel interface and add it to the complementary phase ramps *PHASE_ODD* and *PHASE_EVEN* in Fig. 5.1. This simple structure can implement a phase modulation of the output carrier completely in the digital domain by dynamically adjusting the phase information at the PA outputs. The conceptual block diagram of an *N*-bits pipelined adder based on flip-flop and latch structures are depicted in Fig. 5.2 and Fig. 5.3 respectively. The area occupied by the standard cells in each of these adders can be estimated according to (5.2) and (5.3).

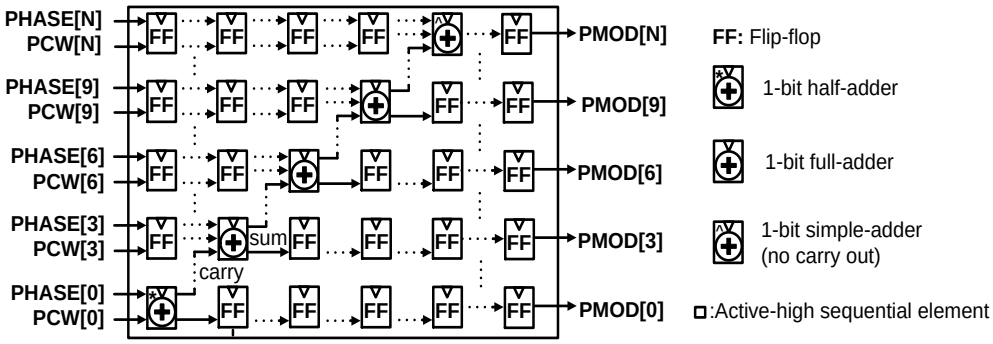


Fig. 5.2. N-bits flip-flop based pipelined adder.

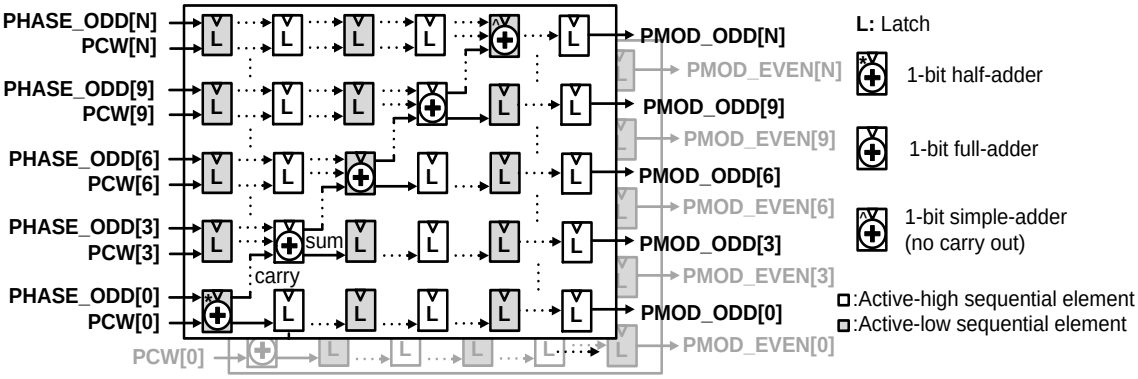


Fig. 5.3. *N*-bits complementary dual-phase latch-based pipeline adder.

$$A_{ADD\_FF} = \left(2N + \left(2N^2 - \sum_{i=1}^{N} i\right) + (N-1)\right) \cdot A_{FF} + NA_{ADDER} \tag{5.2}$$

$$A_{ADD\_L} = 2\left(2N + \left(2N^2 - \sum_{i=1}^{N} i\right) + (N-1)\right) \cdot A_{L} + 2NA_{ADDER} \tag{5.3}$$

$$A_L \approx 0.57 A_{FF} \qquad A_{ADDER} \approx A_{FF} \tag{5.4}$$

Where:

- A_{ADD_FF}: Area of the flip-flop based phase-adder.
- A_{ADD_L}: Area of the latch-based phase-adder.
- A_{ADDER}: Adder area.
- N: Input word length.

The equivalent areas are reported in terms of (×) times the size of a flip-flop cell (A_{FF}). Note that the latch area (A_L) is assumed to be $0.57A_{FF}$ (5.4). Similarly, the adder size in the employed standard cell library is approximately equal to the flip-flop dimensions (5.4). As a result, the pipelined adder dimensions can be expressed in terms

of A_{FF}. The resulting areas when employing different operand sizes are represented in Fig. 5.4. As expected, a penalty is paid when employing the dual-phase complementary sequencing method. However, it should be noticed that, when making use of operands with 12 or more bits, the area of the required cells in the latch-based case never exceeds 20% of the flip-flop based pipelined adder. From (5.2) and (5.3) the number of required flip-flops or latch cells can be determined. A 14-bit phase adder adopting the architecture in Fig. 5.2 contains 328 flip-flop based registers. The total dynamic power consumption of this group follows a distribution with $\mu = 35.6\mu W$ and $\sigma = 1.95\mu W$ when running at 4GS/s (4GHz clock) (Fig. 5.5). On the other hand, a 14-bits latch-based unit following the topology represented in Fig. 5.3 employs 656 registers with a power consumption having a distribution with $\mu = 3.91\mu W$ and $\sigma = 0.34\mu W$ when operating at 4GS/s (2GHz clock) (Fig. 5.6). When increasing the sampling rate up to 8GS/s (4GHz clock), the dynamic energy dissipation of the registers in the same 14-bits latch-based adder can be represented by the distribution in Fig. 5.7. It should be noticed that, when both systems are synchronized with a 4GHz clock, a reduction of about 4.6 times in the median value of the energy consumption can be obtained. However, since the clock distribution becomes more complicated in the latch-based case, the total power consumption in both adders reaches similar values (11 clock tree buffers in Fig. 5.8 and 21 clock tree buffers in the latch-based design (Fig. 5.8 and Fig. 5.9)).

In the flip-flop based design, the dynamic power dissipated in the registers is the dominant contribution to the total power consumption. On the other hand, the energy dissipated in the clock distribution network is the determining factor in the latch-based adder. The leakage power is slightly higher in Fig. 5.9 (258.11μW) compared to Fig. 5.8 (206.67μW) because of the increased number of employed cells. In both cases, the power dissipated in the combinational logic is minimal when compared with the synchronous cells. The maximum sampling rate that could be achieved in a flip-flop based 14-bits adder was 4.13GS/s by simulation. On the other hand, the latch-based core achieved 8.03GS/s under the same conditions. The most important outcome when employing the complementary dual-phase latch-based architecture is an increase by almost a factor of two in the system throughput with only a 26% growth in the occupied area (including the standard cells area, the clock tree and the routing overhead) and a reduction of nearly 4.5% in the power consumption (Fig. 5.10). The phase resolution (θ) can be calculated from (5.5). Since the *PCW* length is 14 bits, the θ_{min} is 0.022°. The required latency to generate a continuous sequence of phase-shifted values is equal to 7½ clock periods (15 interleaving operations).

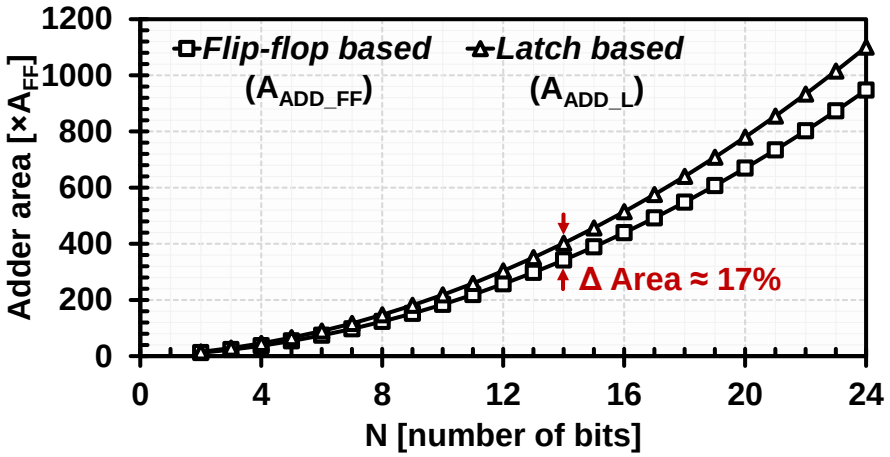


Fig. 5.4. Estimated areas of different pipelined adder circuits.

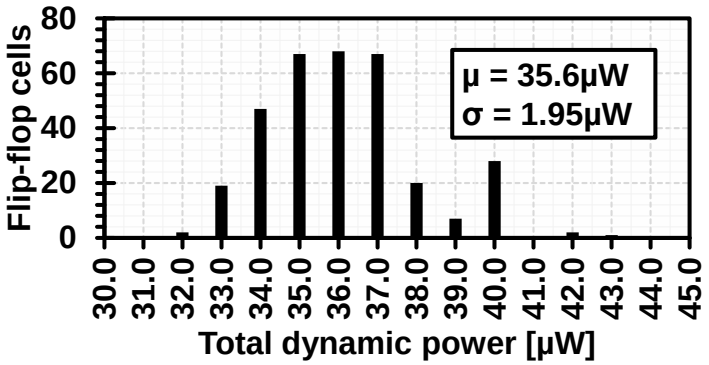


Fig. 5.5. 14-bits flip-flop based adder. Dynamic power distribution of individual registers when running at 4GS/s.

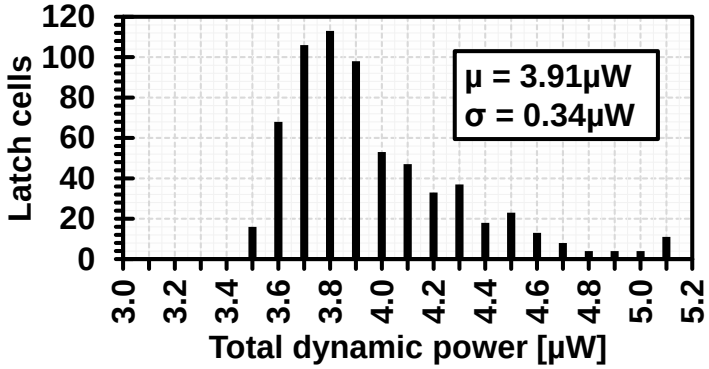


Fig. 5.6. 14-bits complementary dual-phase latch-based adder. Dynamic power distribution of individual registers when running at 4GS/s.

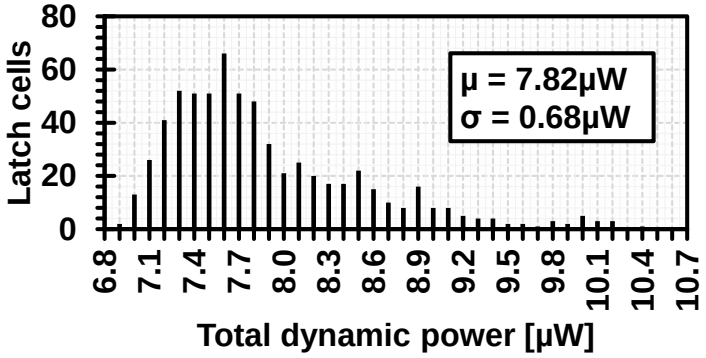


Fig. 5.7. 14-bits complementary dual-phase latch-based adder. Dynamic power distribution of individual registers when running at 8GS/s.

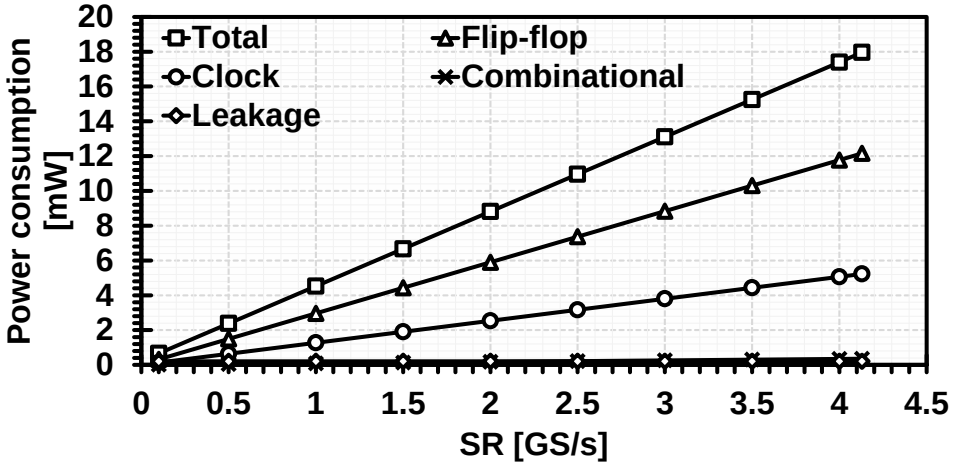


Fig. 5.8. Power breakdown. 14-bits flip-flop based pipelined adder implemented in 65nm CMOS standard cell technology.

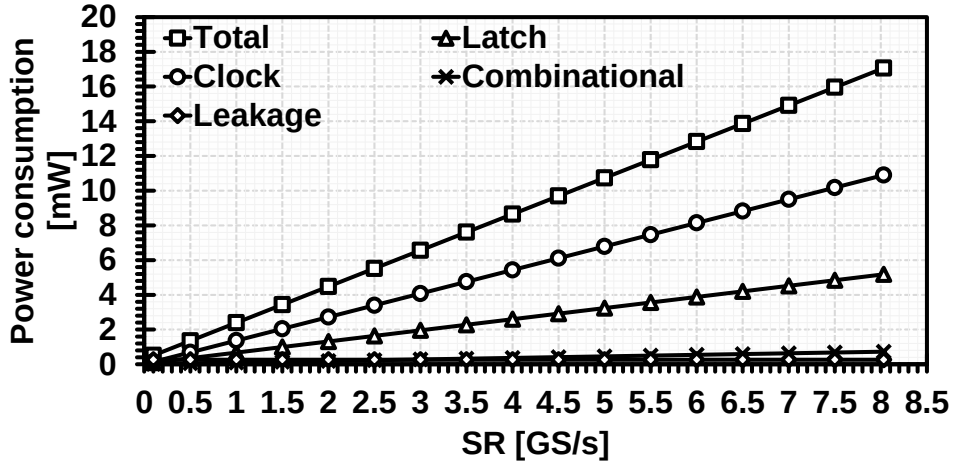


Fig. 5.9. Power breakdown. 14-bits complementary dual-phase latch-based pipelined adder implemented in 65nm CMOS standard cell technology.

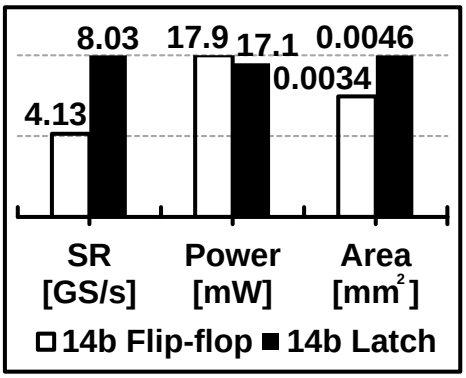


Fig. 5.10. Post layout simulation results.

$$\theta = \frac{PWC \cdot 360°}{2^{14}} \qquad \theta_{\min} = 0.022° \tag{5.5}$$

5.2 High-speed amplitude-multiplier

As represented in Fig. 1.6, no design in region III has addressed the issue of integrating an efficient amplitude-multiplier in a high-speed DDFS architecture. The reason becomes evident when realizing that most of the high-speed synthesizers reported up to date relies on AM-DDFS or NLD-DDFS architecture which are intrinsically unable of implementing AM in the digital domain. Since in this work an NCO core operating at 6.8GS/s has been developed, the next natural step is to incorporate the amplitude modulation capabilities. A structure based on 2-input AND gates is commonly employed to directly generate the partial products in high-performance multipliers [70]. This architecture is often called parallel multiplier and is represented in Fig. 5.11 a) (purely combinational) and 5.11 b) (pipelined, registers are represented as red lines inserted in between the combinational logic). One advantageous property of this multiplier over other methods [71] is its simple structure. It only consists of AND plus adder cells arranged in a feed-forward structure. This fact makes it an ideal candidate for being speed-up by using pipelining and the complementary dual-phase latch-based sequencing method. Also, since in DDFS applications a full-precision multiplication is not often required, the structures for generating the bits in the LSB section (*P(0)* to *P(N-1)* in Fig. 5.11 a)) can be saved (Fig. 5.11 b)). The area occupied by the combinational logic in a $N \times N$ parallel multiplier like the one represented in Fig. 5.11 a) can be estimated by using (5.6). Also, the area occupied by the registers when pipelining the partial product stages with flip-flop cells can be determined as in (5.8). This equation accounts the registers employed to pipeline the LSB section (*P(0)* to *P(N-1)* in Fig. 5.11 a)).

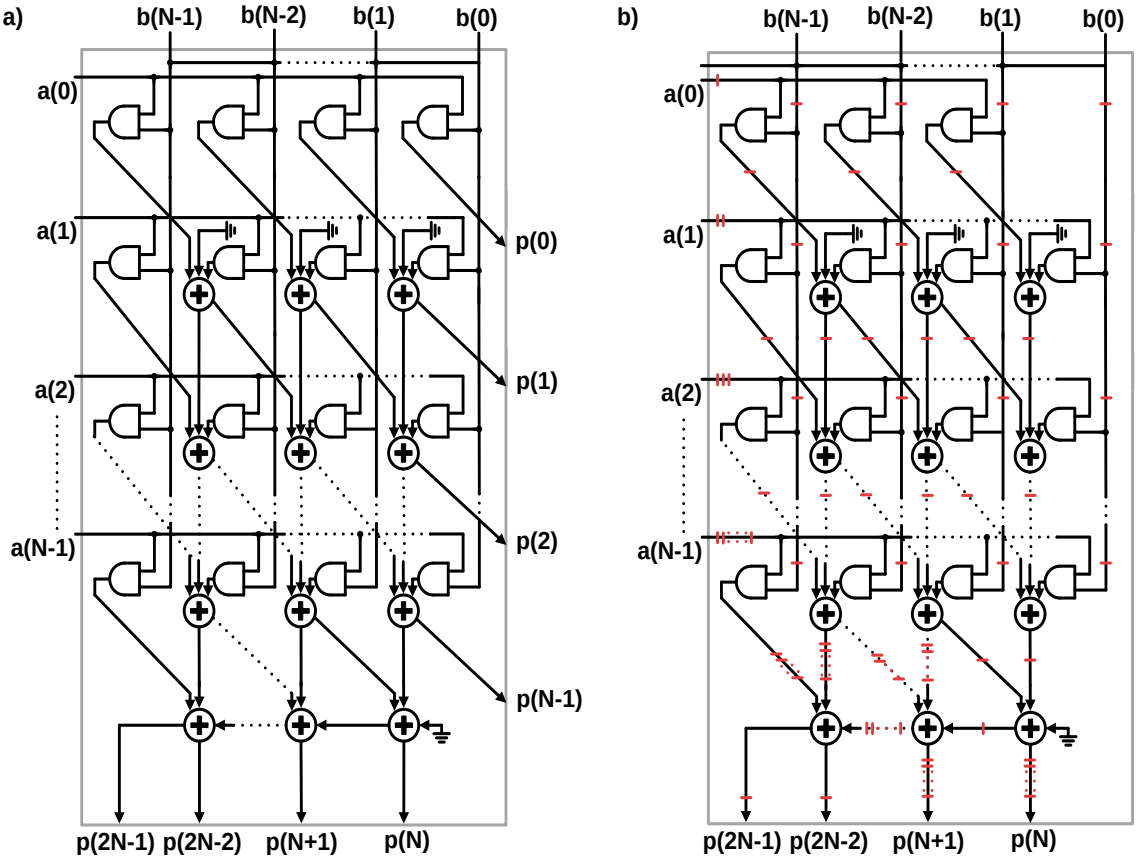


Fig. 5.11. Parallel multiplier architectures. a) 2×*N*-bits precision. Non-pipelined. b) *N*-bits precision pipelined.

$$A_{MULT\_COMB} = N^2 A_{AND} + \left(N^2 - N\right) A_{ADDER} \tag{5.6}$$

$$A_{AND} \approx 0.3 A_{FF} \qquad A_{ADDER} \approx A_{FF} \tag{5.7}$$

Where:

- A_{MULT_COMB}: Area occupied by the combinational logic.
- A_{AND}: Area of the AND cell.
- N: Input words length.

$$A_{MULT\_FF} = \left(6N^2 - 2N + 2 - 3\left(\sum_{i=1}^{N-1} i\right)\right) A_{FF} \tag{5.8}$$

Where:

- A_{MULT_FF}: Area occupied by the flip-flops in an $N \times N$ multiplier.

In case only half-resolution is required, (5.8) becomes:

$$A_{MULT\_F} = \left(6N^2 - 6N + 2 - 2\left(\sum_{i=1}^{N-1} i\right)\right)A_{FF} \tag{5.9}$$

Hence, the total area occupied by the logic (sequential and combinational) in Fig. 5.11 b) can then be approximated as:

$$A_{MULT\_TOTAL} = \left(\left(6N^2 - 6N + 2 - 2\left(\sum_{i=1}^{N-1} i\right)\right)A_{FF}\right) + \left(N^2 A_{AND} + \left(N^2 - N\right)A_{ADDER}\right) \tag{5.10}$$

Where:

- A_{MULT_TOTAL}: Area of the flip-flop based amplitude-multiplier (half-resolution).

The equivalent area of different half-resolution multipliers is reported in terms of (×) times the size of a flip-flop cell (A_{FF}) in Fig. 5.12. It should be noticed how when implementing a 10×10-bit multiplier, 190 combinational cells (100 AND plus 90 1-bit adders) are required. The number of flip-flops needed when applying pipeline to this architecture is 452 (5.9). A similar graph can be obtained when using the complementary dual-phase latch-based sequencing method in the pipeline structure (Fig. 5.13). Equation (5.10) now results in (5.11) because of the needed duplicated logic and complementary latch pairs.

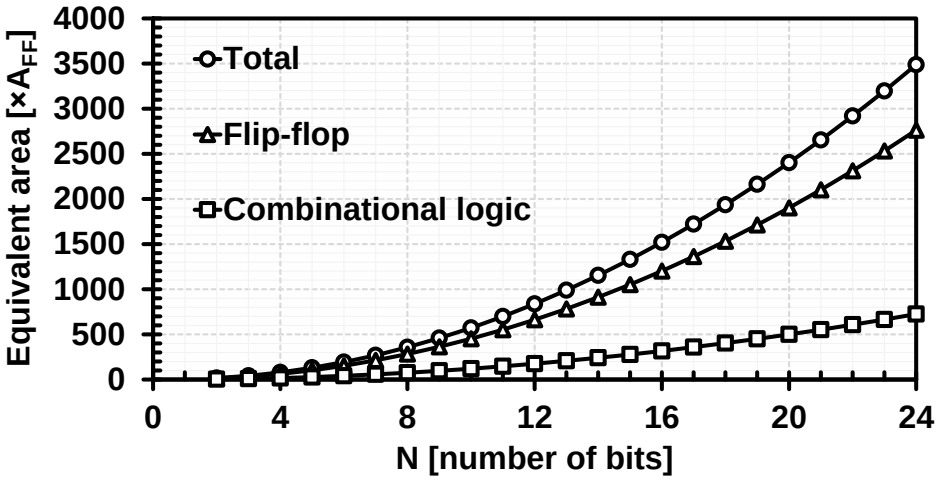


Fig. 5.12. Equivalent area of different $N \times N$ half-resolution parallel multipliers. Flip-flop based pipelining.

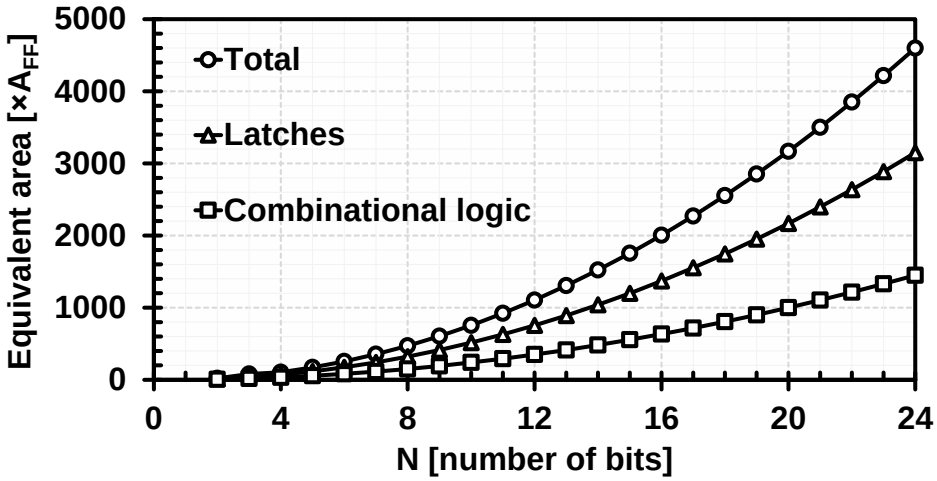


Fig. 5.13. Equivalent area of different $N \times N$ half-resolution parallel multipliers. Latch-based pipelining.

As expected, an increase in the total equivalent area can be observed when comparing Fig. 5.13 and Fig. 5.12. This is due to the required duplicated combinational logic and the substitution of the flip-flops by a complementary pair of latches.

$$A_{MULT\_TOTAL} = 2A_L\left(6N^2 - 6N + 2 - 2\left(\sum_{i=1}^{N-1} i\right)\right) + 2\left(N^2 A_{AND} + \left(N^2 - N\right)A_{ADDER}\right) \quad (5.11)$$

A 10×10-bits parallel multiplier employing the complementary dual-phase latch-based method can be represented as in Fig. 5.14. The structure is also divided into mirrored layers having a 180° phase offset among equivalent data transitions in order to equal the maximum throughput of the NCO channel. The operands are the *ACW* (10-bits) and the *SINE_ODD/EVEN* outputs from the PAC (10-bits). This feedforward architecture only requires 1-bit full-adders and AND gates based on static CMOS logic to perform the multiplication operations. Pre-skewing and post-skewing latches are also employed in order to pipeline the logic through the multiplication channel at the required sampling rate. It should be noticed that the intermediate arithmetic calculation results (carry and sum terms) are interleaved among the complementary layers. Hence, a new operation is executed during both high and low levels of the clock (different colored arrows in Fig. 5.14). The final stage of this multiplier unit is implemented as a 9-bits pipelined ripple-carry adder also featuring a complementary dual-phase latch-based pipeline array. This system exhibits a 9½ clock periods latency resulting from 19 interleaved operations during different levels of the clock. The dynamic power consumption of the register cells employed in two different 10×10-bits multipliers adopting the architectures in Fig. 5.11 b) and Fig. 5.14 are represented in Fig. 5.15 to Fig. 5.17. The energy dissipated by the flip-flops in a 10×10 pipelined parallel

multiplier follows a distribution with μ = 34.74μW and σ = 2.82μW when operating at the maximum sampling rate (3.98GS/s) in the employed 65nm CMOS technology (Fig. 5.15). At the same sampling rate, the energy dissipated by the latches in a complementary dual-phase multiplier also having 10-bits operands can be represented by the distribution in Fig. 5.16. When running at 7.87GS/s (maximum *SR* by simulation) it follows a distribution with μ = 7.56μW and σ = 1.44μW (Fig. 5.17).

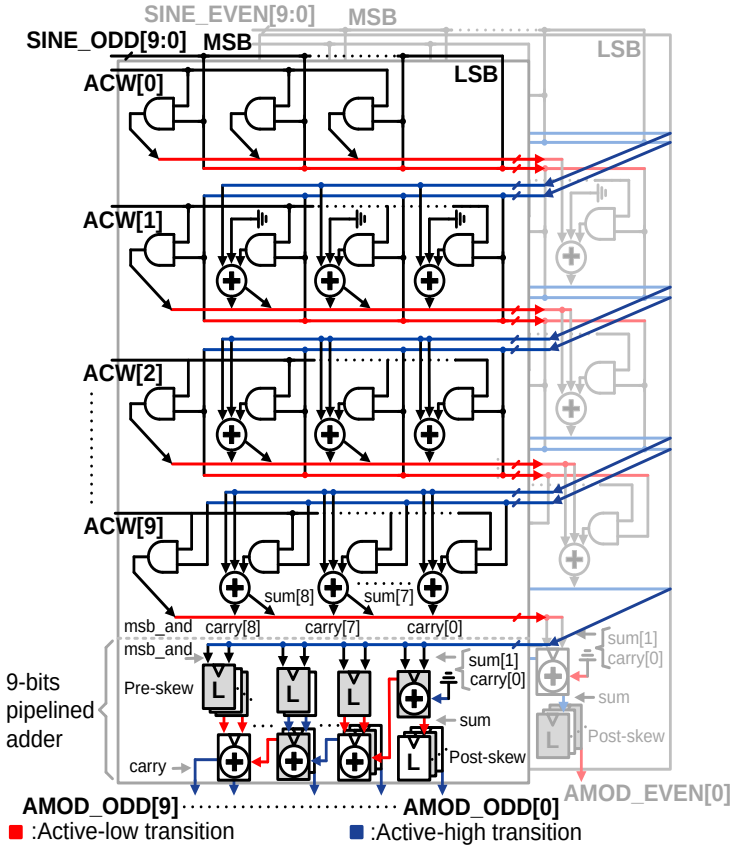


Fig. 5.14. 10×10-bits parallel multiplier employing the complementary dual-phase latch-based method.

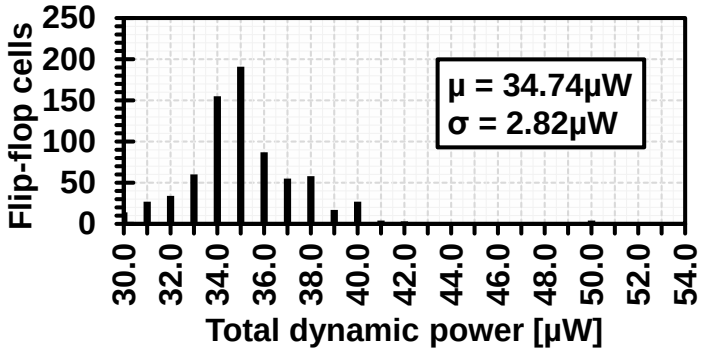


Fig. 5.15. Dynamic power consumption of the register cells in a 10×10-bits half-resolution multiplier. Flip-flop based pipelined architecture. *SR*= 3.98GS/s.

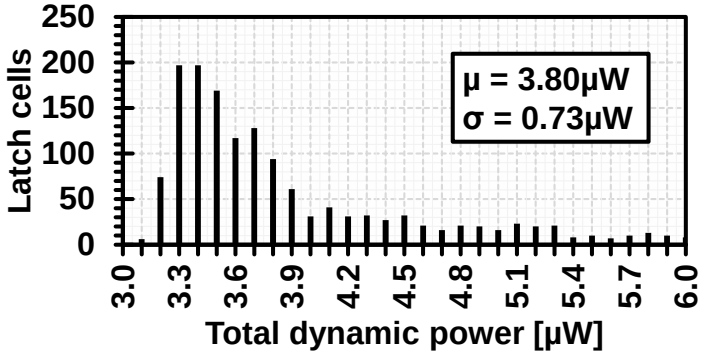


Fig. 5.16. Dynamic power consumption of the register cells in a 10×10-bits half-resolution multiplier. Latch-based pipelined architecture. *SR*= 3.98GS/s**.**

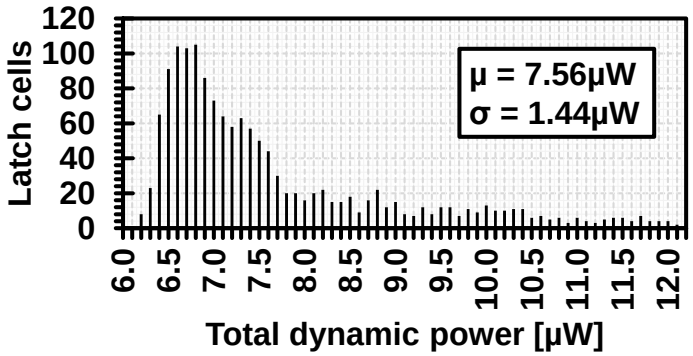


Fig. 5.17. Dynamic power consumption of the register cells in a 10×10-bits half-resolution multiplier. Latch-based pipelined architecture. *SR*=7.87GS/s.

A reduction of about 9.1 times in the median value of the energy consumed in the registers can be obtained by employing latches when both systems run at equivalent sampling rates. The latch-based system can achieve 4.6 times smaller median value when compared to the flip-flop based case even when running at almost twice the sampling rate. The power breakdown when using both synchronization methods is represented in Fig. 5.18 and Fig. 5.19. In the flip-flop based case, the main power contribution comes from the internal energy consumption of the registers. On the other hand, the clock distribution network is dominant in the latch-based design. Consequently, the total power dissipated when running at maximum sampling rate is roughly 38.5mW in both cases. However, the latch-based architecture can achieve twice the throughput when compared with the flip-flop topology. The post-layout simulation data is reported in Fig. 5.20. When employing a 10-bits multiplier, the minimum amplitude resolution that can be achieved is 1.17mV whit an output swing of $1.2V_{pp\text{-}diff}$. The modulated amplitude levels can be determined according to (5.12).

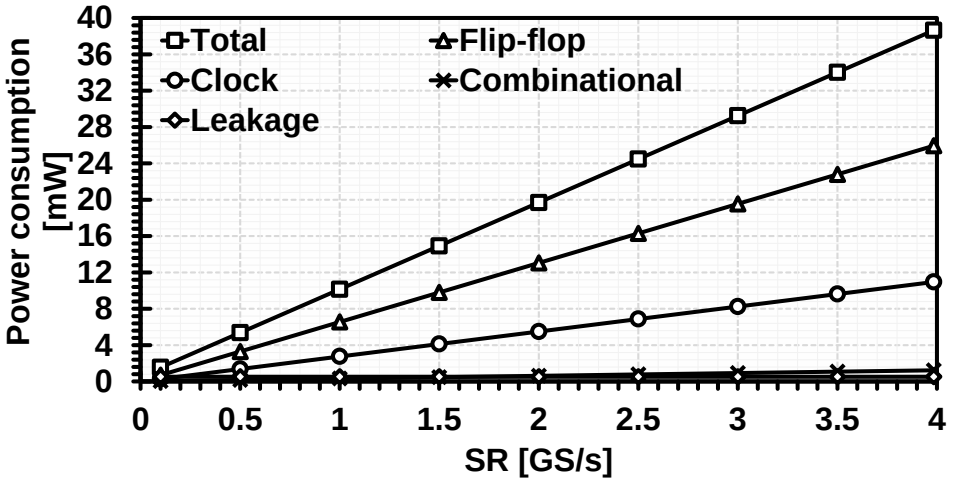


Fig. 5.18. Power breakdown. 10-bits half-resolution parallel multiplier. Flip-flop based architecture.

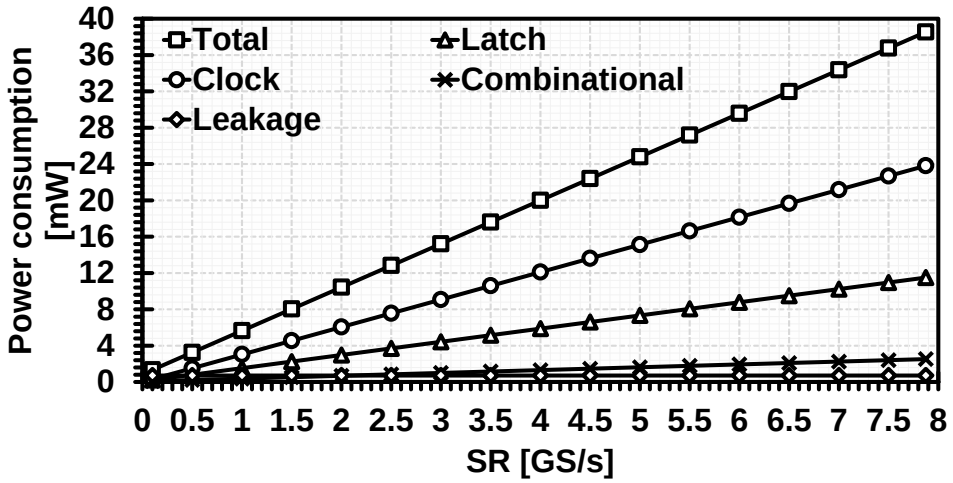


Fig. 5.19. Power breakdown. 10-bits half-resolution parallel multiplier. Latch-based architecture.

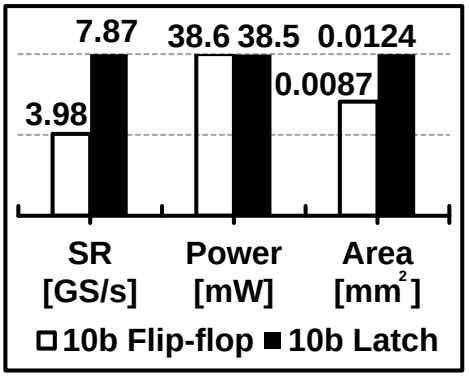


Fig. 5.20. Post-layout simulation results.

$$A = \frac{ACW \cdot 1.2V_{pp-diff}}{2^{10}} \qquad A_{\min} = 1.17mV \tag{5.12}$$

5.3 Design verification

Static timing, power and area analysis were performed by employing Synopsys/Design-Compiler/IC-Compiler toolset. Behavioral, post-synthesis and post-layout simulation were completed with Mentor Graphics/ModelSim and Cadence/NCsim. The post-layout simulated operation when implementing an on-off keying (OOK) modulation is represented in Fig. 5.21. The represented waveforms correspond to the *AMOD_ODD* and *AMOD_EVEN* signals in Fig. 5.1 when the *FCW1* in Table 5-1 is selected and the system is running at 6.8GS/s. The output waveforms when implementing a binary phase shift keying (BPSK) modulation were also simulated under the same conditions. The signals represented in Fig. 5.22 corresponds to consecutive 180° phase shifts in the output carrier.

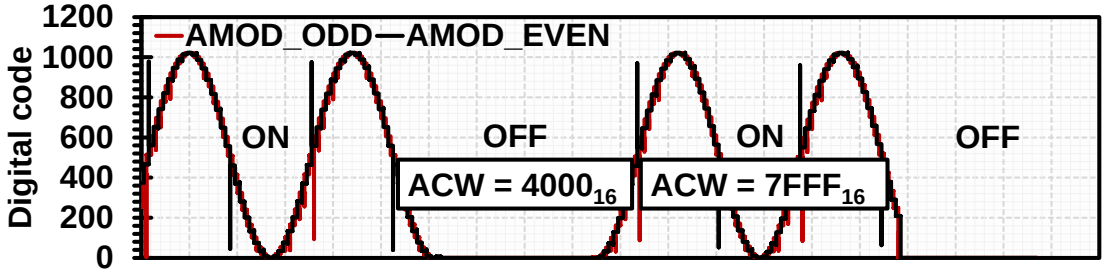


Fig. 5.21. F_{OUT} = 99.92MHz. Output carrier being OOK modulated at 6.8GS/s.

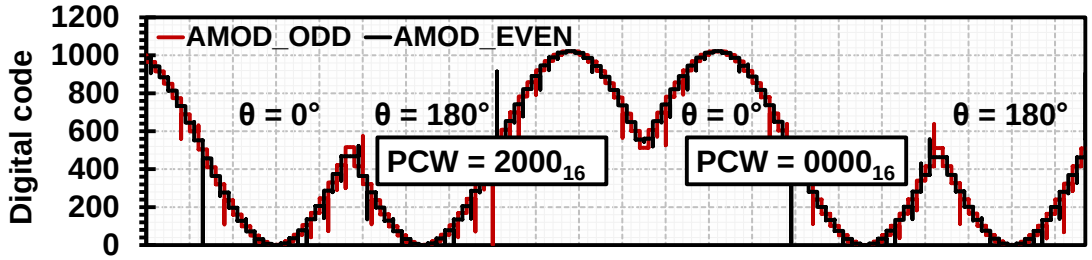


Fig. 5.22. F_{OUT} = 99.92MHz. Output carrier being BPSK modulated at 6.8GS/s.

5.4 Summary of the solutions for high-speed digital modulations

In this chapter, high-speed architectures for a phase-adder and an amplitude multiplier has been discussed. The relevant design equation has been presented and the simulated results were also introduced. The throughput of the modulation structures

exceeded the required sampling rate in the NCO core (6.8GS/s) by employing the complementary dual-phase latch-based sequencing method. A 14-bits phase-adder capable of running at 8.03GS/s by simulation while consuming 17.1mW is reported. Similarly, the implemented 10×10-bits amplitude-multiplier consumes 38.5mW at 7.87GS/s. This solution can be integrated with the NCO core described in Chapter 3 and the 2I-RDAC unit presented in Chapter 4 in order to implement a high-speed DM-DDFS architecture having FM, PM and AM capabilities in CMOS technology.

CHAPTER 6:
PROOF-OF-CONCEPT CHIPS

THREE proof-of-concept chips were implemented in 65nm CMOS technology in order to demonstrate the merits of the proposed design approach. Each of the implementations targeted specific features. To begin, a 2GS/s synthesizer consuming only 59mW/(GS/s) is described. The sampling rate achieved with this prototype equals the maximum throughput reported in previous CMOS implementations [9]. Moreover, this design attains a record power efficiency when compared with other silicon-based designs. This constitutes the distinctive characteristic of the first evaluated chip and at the same time highlights the merits of the employed complementary dual-phase latch-based sequencing method in terms of power efficiency [47]. A second attempt targeted a higher throughput operation by integrating a 2I-RDAC core. The benefits of the proposed design methodology are evidenced by achieving the first CMOS-based DDFS running at 7GS/s [48]. Finally, the FM, PM and AM capabilities were integrated into a complete-DDFS-solution. As a result, the only DDFS supporting 7GS/s and featuring frequency, phase and amplitude modulations is demonstrated in this chapter [49].

The employed measurement setup is represented in Fig. 6.1. The evaluation procedures get considerably simplified because in all cases complete-DDFS-solutions were integrated. In that way, only digital settings need to be configured and the device under test (DUT) output can be directly measured from an evaluation board prepared for that purpose.

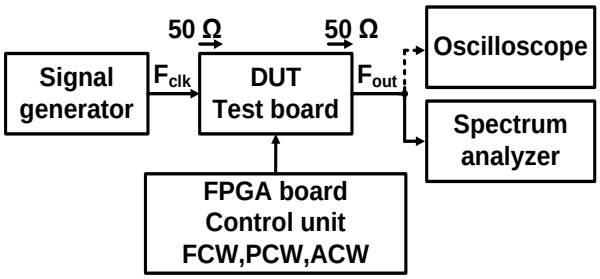


Fig. 6.1. Measurement setup.

Further simplification was achieved by pre-storing default *FCW*s in the on-chip registers. The system controller and the baseband signal processing unit employed to evaluate the solution in [49] were implemented in FPGA devices. External 1:1 baluns were used in all cases to conform single-ended output signals suitable for driving the recording instruments. More than 3 samples were measured at room temperature in all the experiments. The collected data was post-processed and averaged results are reported in the following sections.

6.1 A 2GS/s 118mW DM-DDFS in 65nm CMOS technology

The block diagram of this DDFS solution is represented in Fig 6.2. The NCO core described in Chapter 3 is integrated with a conventional RDAC circuit. The waveform samples (*SINE_ODD* and *SINE_EVEN* in Fig. 6.2) are multiplexed before inputting the data to the DAC. A 10-bits, voltage-mode RDAC was employed in order to implement a proof-of-concept prototype (Fig. 6.3). The MSB section is a 6-bits thermometer-coded RDAC and the LSB segment is derived from a 4-bits R-2R ladder network.

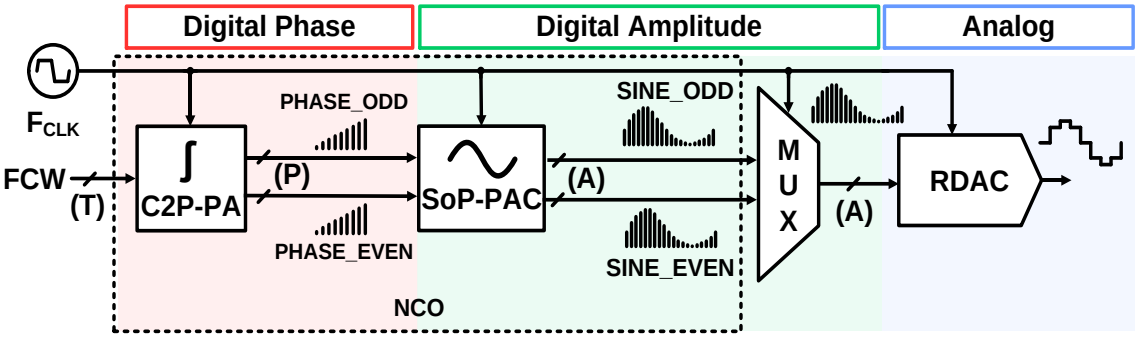


Fig. 6.2. 2GS/s DM-DDFS block diagram.

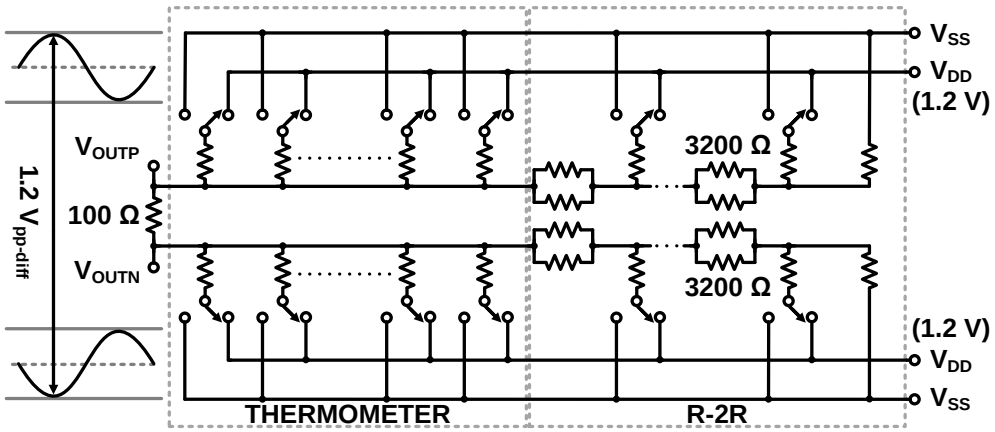
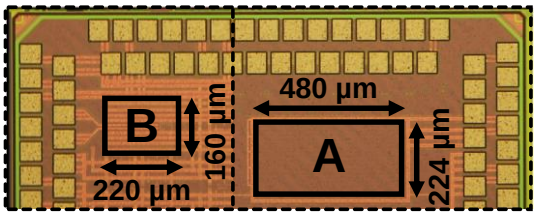


Fig. 6.3. Voltage-mode RDAC.

The circuit was designed by using unsilicided P+ polysilicon resistors and NMOS/PMOS pass-gates (PG) as switches. The differential output impedance and amplitude swing are 50Ω and $1.2V_{pp\text{-}diff}$ respectively when terminated with a 100Ω off-chip resistance. As previously discussed, this type of DAC is not limited by the voltage headroom reduction along with transistor size scaling and lowering of power supply voltage. Besides proper layout, no other high-speed techniques like interleaving or reduced-swing drivers were used.

6.1.1 Implementation

A test chip was fabricated in a 1P9M 65nm CMOS process (Fig. 6.4). An evaluation board was also developed by employing glass-reinforced epoxy laminate substrate (FR-4) and prototypes encapsulated in a 144-pin low-profile quad flat package (LQFP). The reference clock signal was driven by an R&S SML02 signal generator. A U3751 spectrum analyzer from Advantest and a Tektronix MSO4104 mixed signal oscilloscope were also employed. All the measurements were performed by taking the unfiltered single-ended output signal from a 1:1 balun connected after the 100Ω off-chip resistance. The measured performance of the DM-DDFS is reported in Table 6-1 and the following subsections.



REFERENCE	CORE	AREA
A	NCO	0.11mm²
B	RDAC	0.03mm²

Fig. 6.4. Die micrograph. 2GS/s solution**.**

TABLE 6-1: EXPERIMENTAL RESULTS

Reference	Max. SR [GS/s]	Active area [mm²]	Power consumption [mW]
NCO	2	0.107	72
RDAC		0.035	46
NCO + RDAC		0.142	118

6.1.2 Device characterization

The W-SFDR performance is plotted from DC to Nyquist frequency when the DM-DDFS operates at maximum sampling rate in Fig. 6.5. The registered values were better than 41dBc up to 750MHz and 30dBc over the entire Nyquist bandwidth. Fig. 6.6 and Fig. 6.7 illustrate the SFDR boundaries when the DM-DDFS operates at 2GS/s. Fig.

6.8 and Fig. 6.9 show the time domain measurements under equivalent conditions and without compensating the cables and balun insertion losses. The energy performance versus the output frequency is represented in Fig. 6.10.

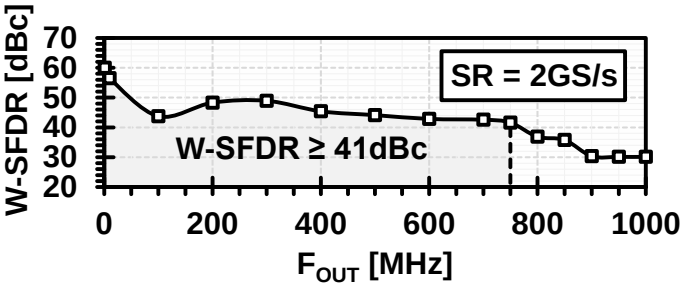


Fig. 6.5. W-SFDR vs DM-DDFS output frequency.

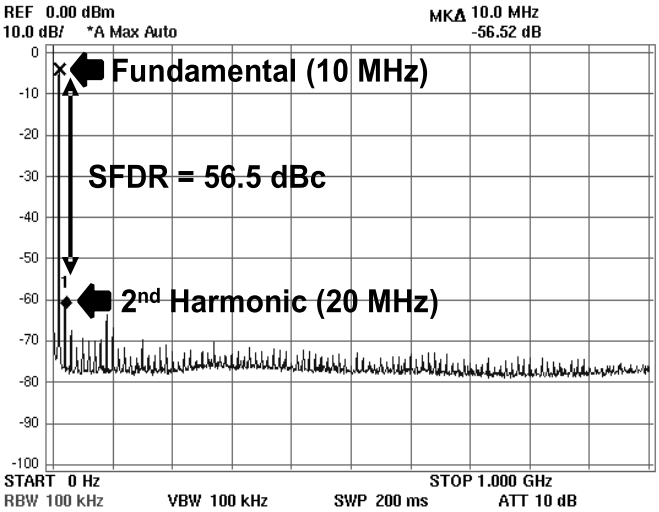


Fig. 6.6. Best case W-SFDR. F_{CLK} = 1GHz. *SR* = 2GS/s.

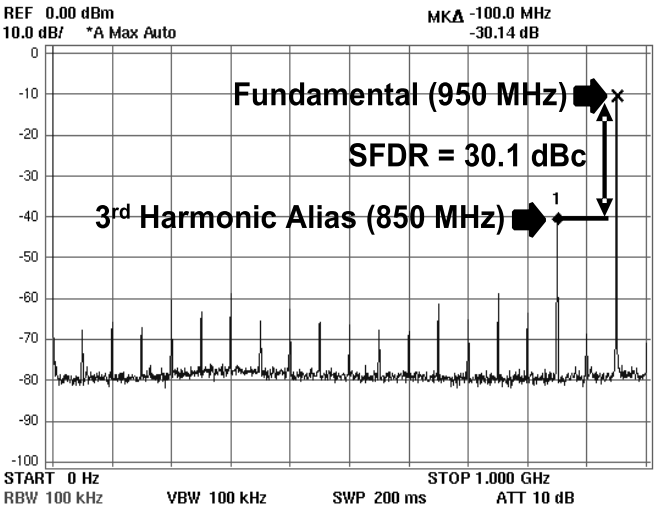


Fig. 6.7. Worst case W-SFDR. F_{CLK} = 1GHz. *SR* = 2GS/s.

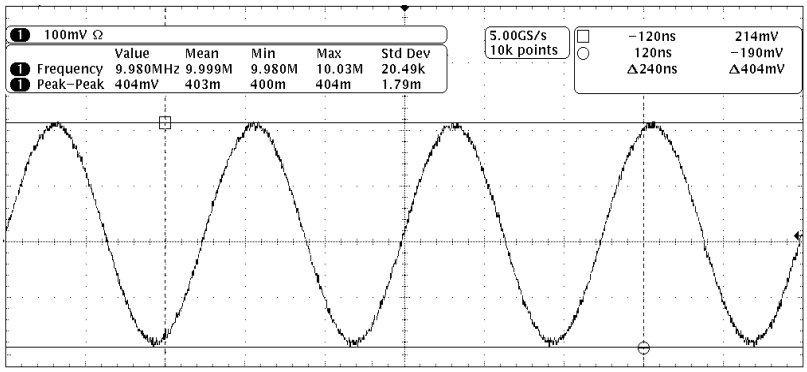


Fig. 6.8. DM-DDFS output waveform. F_{OUT}= 10MHz. *SR* = 2GS/s.

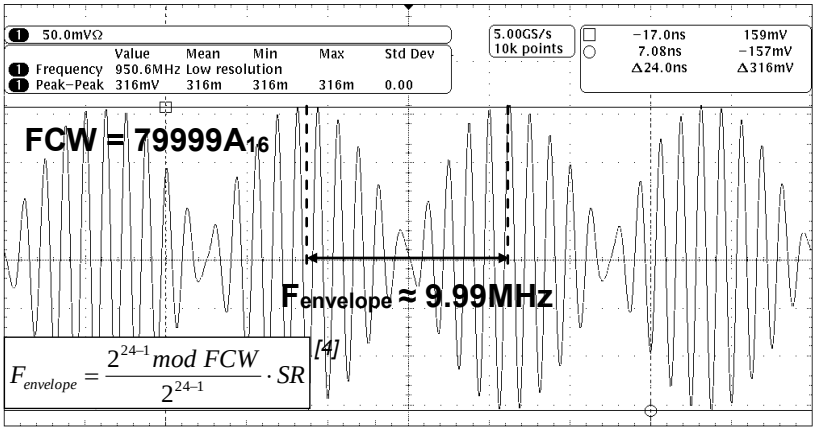


Fig. 6.9. DM-DDFS output waveform. F_{OUT}= 950MHz. *SR* = 2GS/s.

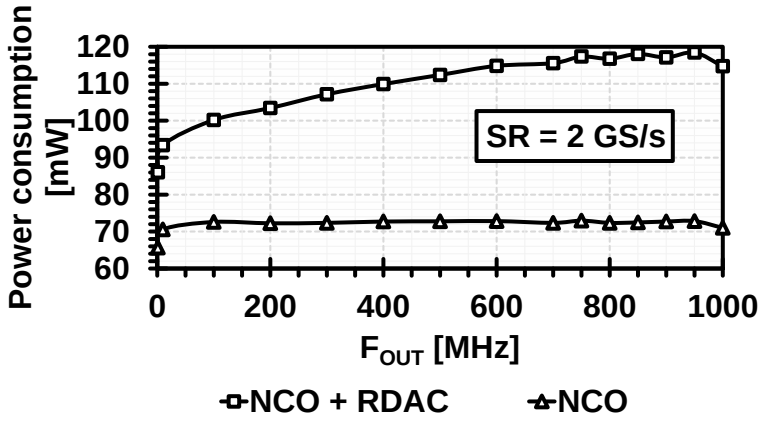


Fig. 6.10. Power consumption vs. DM-DDFS output frequency**.**

The PA block only consumes 2.6mW when running at the maximum sampling rate. This fact highlights the merits of the implemented complementary dual-phase latch-based phase accumulator in terms of power efficiency. The PAC block dissipates 51.4mW when operating at 2GS/s. This value represents 43.5% of the total power

consumption (NCO + RDAC) in Table 6-1.

6.1.3 Performance comparison

Table 6-2 lists those measured DDFSs attaining higher power efficiency according to the survey conducted in this work.

TABLE 6-2: PERFORMANCE COMPARISON

Reference	This Work	JSSC'14 [9]	RFIC'09 [72]	MWCL'08 [73]
Architecture	DM-DDFS	NLD-DDFS	AM-DDFS	AM-DDFS
Technology	65nm CMOS	55nm CMOS	0.35µm SiGe	0.25µm SiGe
FCW width [bits]	24	32	8	9
Amplitude Resolution [bits]	10	9	6	8
Worst case W-SFDR [dBc]	30(1)	55.1(2)	20(2)	18(3)
Active area [mm²]	0.142	0.1	1.15(4)	0.42
SR [GS/s]	2	2	15	6
PE [mW/(GS/s)]	59	65	24.4	51.3
FoM (5)	542	8944	413	156

(1) *Packaged* (2) *Die-on-board* (3) *Wafer* (4) *With pads* (5) $FoM = \frac{2^{SFDR_{worst}[dBc]/6} \cdot SR[GS/s]}{P_{\max}[W]}$ *[9]*

Fig. 6.11 represents the state of the art of this technology including this work. The best timing performance and FoM among previous CMOS-based DDFSs were disclosed in [9]. To the extent of our knowledge, the finest PE has been reported in [72]. An AM-DDFS running at 6GS/s while consuming 51.3mW/(GS/s) was described in [73]. In terms of power efficiency, this work benchmarks favorably against all CMOS implementations in Table 6-2 and Fig. 6.11. Compared with [72] and [73], this circuit has superior frequency and amplitude resolutions. It is also fabricated by using a standard CMOS process instead of the more costly SiGe alternative. Moreover, the second best FoM among designs consuming less than 65mW/(GS/s) [9], [72], [73] was achieved. Finally, contrasting with references in Table 6-2, amplitude modulation can be further implemented in the digital domain when using the proposed DM-DDFS architecture. It should be noted that the maximum operating frequency and W-SFDR of this system were limited by the employed RDAC. Post-layout back-annotated simulation results showed that the previously described NCO core can operate in excess of 6GS/s. Also, unlike in [9], [72], [73], all the measurements were carried out by employing an evaluation board including packaged prototypes. Therefore, results are considered affected by the bonding wires and interconnection parasitics.

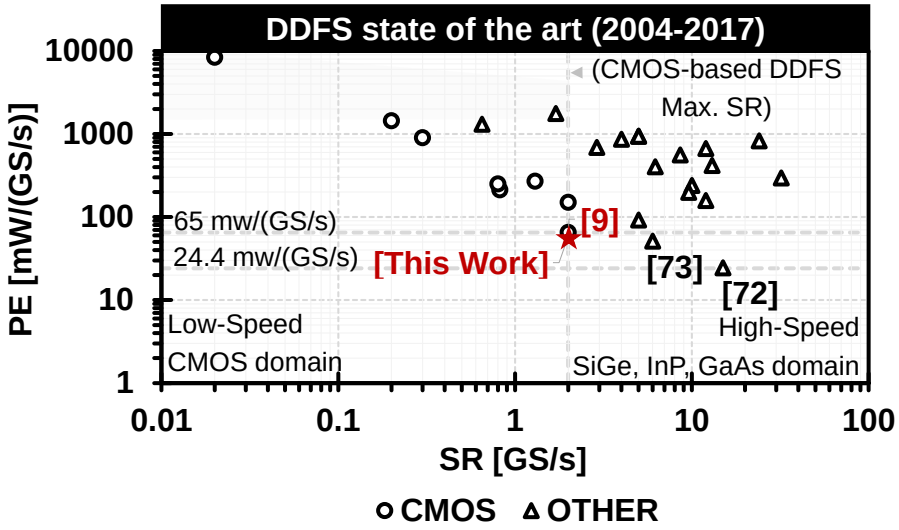


Fig. 6.11. Power efficiency vs. sampling rate.

6.1.4 Summary of a 2GS/s 118mW DM-DDFS in 65nm CMOS

A proof-of-concept frequency synthesizer has been fabricated and characterized in 65nm CMOS technology. A complementary dual-phase latch-based architecture including a phase to amplitude converter made from pipelined SoP terms and a 24-bits phase accumulator has been implemented. These techniques improve the state of the art of DM-DDFSs by enabling a power efficiency of 59 mW/(GS/s) while operating at 2 GS/s. Since this is a digitally intensive solution intended for radio-frequency signals generation, potential improvements in energy efficiency are expected when moving to a more advanced CMOS technology process.

6.2 A 7GS/s DM-DDFS with a two-times interleaved RDAC in 65nm CMOS technology

The block diagram of this DDFS solution is represented in Fig 6.12.

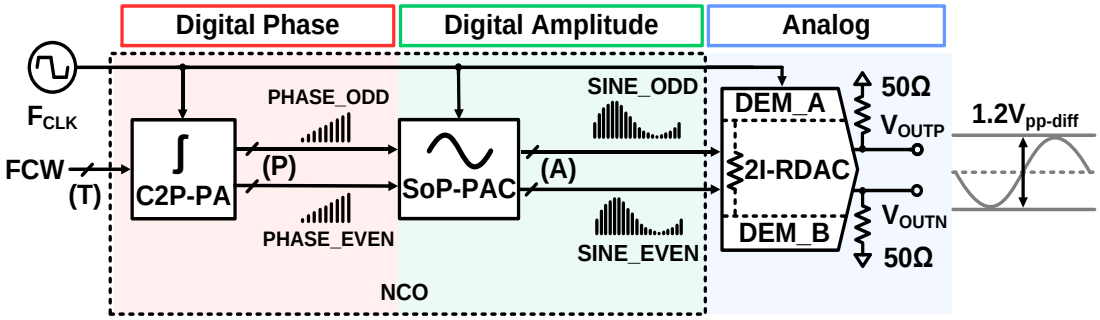
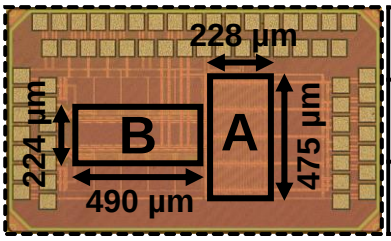


Fig. 6.12. 7GS/s complete-DDFS-solution.

The NCO core described in Chapter 3 is integrated with the 2I-RDAC presented in Chapter 4. The most important features incorporated in this solution are its inherent high-speed operation and the integration of an RSTC-DEM core (DEM_A & DEM_B) in order to improve the N-SFDR performance.

6.2.1 Implementation

A proof-of-concept chip was fabricated in a 1P9M 65nm CMOS process (Fig. 6.13). Both the NCO and the 2I-RDAC cores occupy an active area of about 0.11mm^2. The prototypes were encapsulated in an LQFP-144 package and assembled in an evaluation board made of FR-4 (Fig. 6.14). The total chip die area is 0.88×1.460mm^2, including a clock divider/distribution unit, the I/O pads, an array of internal decoupling capacitors and the dummy filling elements. All the digital logic was designed by using standard-cell technology and a fully synthesizable flow including automatic place and route. The Design-Compiler tool in topographical mode was employed during the synthesis step. This tool can predict the post-layout delay information by using more realistic interconnection parasitics. Consequently, the correlation between the post-synthesis and post-layout quality of results is improved.



REFERENCE	CORE	AREA
A	NCO	0.11 mm^2
B	2I-RDAC	0.11 mm^2

Fig. 6.13. Die micrograph. 7GS/s DM-DDFS solution.

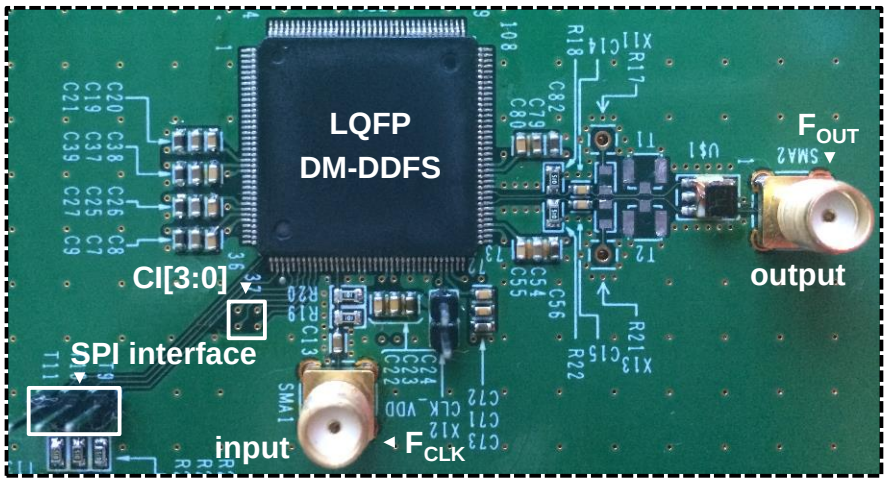


Fig. 6.14. Evaluation board.

The clock mesh and the RDAC cells were laid out manually, minimizing the length of the current-carrying paths, and using redundant vias and contacts. The R-2R and THERMOMETER sections were implemented by employing unsilicided P^+ polysilicon resistors with a $3.3\times12.43\mu m^2$ area. The output frequency can be configured via a serial peripheral interface. The active *FCW* can be selected among 16 pre-stored values by means of a 4-bits CMOS control interface (CI[3:0] in Fig. 6.14). The clock signal is driven by an Agilent E8257D signal generator. All the measurements were performed by taking the unfiltered single-ended output signal from a 1:1 balun connected after the 50 Ω off-chip resistances. A U3751 spectrum analyzer from Advantest, an Agilent DSO90804A high-performance oscilloscope and an E5052B Signal Source Analyzer from Keysight were also employed.

6.2.2 Device characterization

All the measured prototypes were capable of operating at 7GS/s. This performance exceeds the 6.8GS/s static timing estimation in section 4.3 and can be explained by the 20ps of unintended time borrowing that can be allocated (or reduced from the clock period) without incurring in any timing violation. W-SFDR, N-SFDR (bandwidth ≈ 1.4% of the *SR*), and time domain measurements are reported from Fig. 6.15 to Fig. 17. The W-SFDR (DC to Nyquist frequency) when operating at 7GS/s is plotted in Fig. 6.18. This graph shows the curves corresponding to the measured 2nd (2HD), 3rd (3HD) and 5th (5HD) harmonic distortions falling into the first Nyquist zone (including the alias images). The measured interleaving distortions (ID) and the theoretical 3ps duty cycle error profile (Fig. 2.7) are also displayed in Fig. 6.18. At lower synthesized frequencies ($F_{OUT} \leq 308$MHz) the third harmonic spurs are dominant (gray area). Hence, the measured results follow the 3HD curve. Under these conditions, the interleaving artifacts fall close to the Nyquist frequency and are more attenuated in the balun and RF cables. The remaining points were determined by the interleaving spurs and, therefore, the measured values overlap the ID curve (except at $F_{OUT} = 3.499$GHz (Fig. 6.16) where a non-harmonically related spur dominates the W-SFDR). It should be noticed how in this frequency range ($F_{OUT} \geq 308$MHz) the ID curve (and consequently, also the measured curve) reasonably follows the 3ps duty cycle error profile. At higher synthesized frequencies ($F_{OUT} \geq 2980$MHz), the interleaving spurs move closer to DC and are more attenuated by the uncompensated AC-coupled output interface (Fig. 6.14). For that reason, the W-SFDR exhibits a better performance compared with the theoretical case.

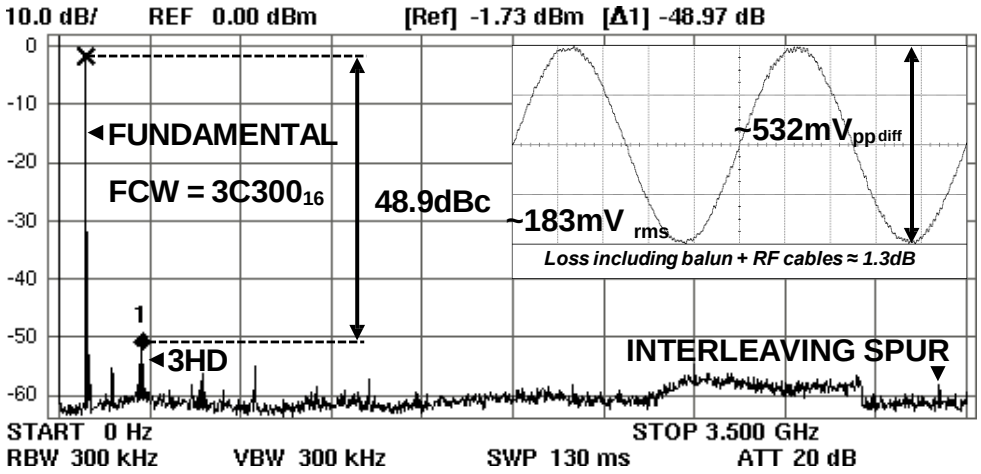


Fig. 6.15. W-SFDR and output waveform. F_{OUT}= 102.8MHz. *SR* = 7GS/s.

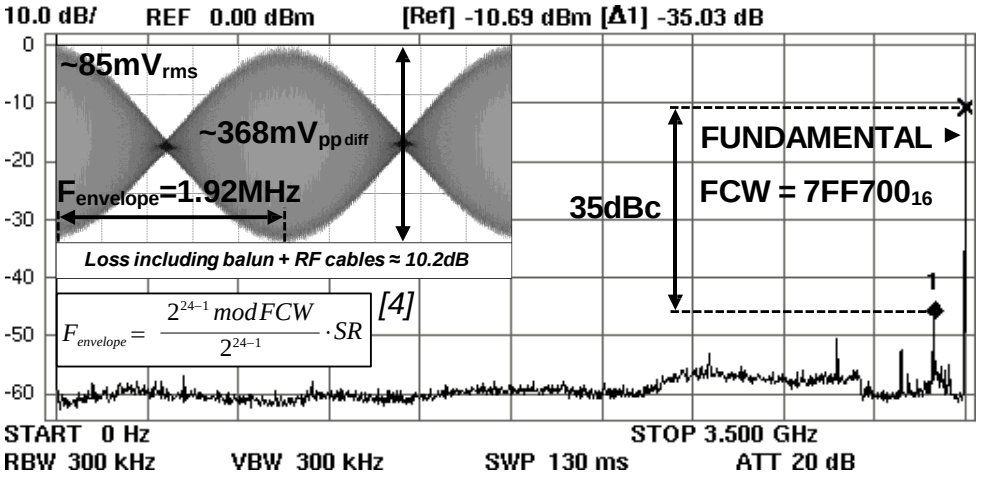


Fig. 6.16. W-SFDR and output waveform. F_{OUT}= 3.499GHz. *SR* = 7GS/s.

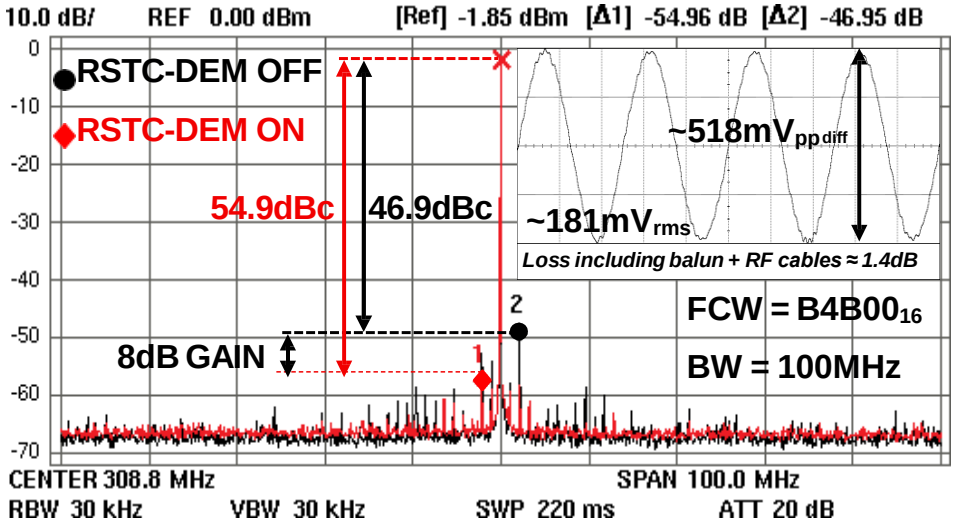


Fig. 6.17. N-SFDR and output waveform. F_{OUT}= 308.8MHz. *SR* = 7GS/s.

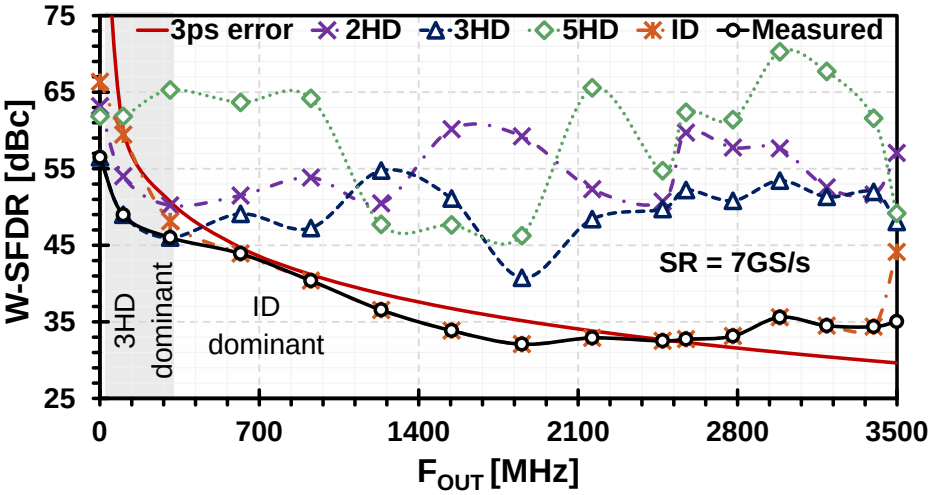


Fig. 6.18. Measured W-SFDR vs DM-DDFS output frequency.

The measured N-SFDR is reported and contrasted with previous arts in Fig. 6.19. The evaluated prototypes exhibit the characteristic sweet-spots among the first Nyquist zone [4], [18]. The N-SFDR of the synthesized carrier reaches 59.2dBc at 926.4MHz (Fig. 6.20). This system can switch between different output frequencies with a latency of about 7.6ns (26 ½ clock periods at 7GS/s) (Fig. 6.21). The full-scale settling time was measured at the differential output to within a 10%, 4% and 2% error bands (Fig. 6.22). The non-idealities in the resistive units together with the bonding wire parasitics (section 2.3), the capacitance of the ESD protection circuit and the load resistance will limit the maximum sampling rate (worst condition, F_{OUT} = 3.499GHz and SR = 7GS/s). This synthesizer is capable of settling in 140ps to within 10% of the nominal full-scale value (600mV$_{pp\text{-}diff}$ when loaded with 50Ω). It should be noticed that, at the typical frequencies of interest for most applications (up to about 40% of the sampling rate in order to relax the antialiasing filter requirements), the voltage step sizes are smaller than the full-scale swing. Hence, the error band to which the system can settle within one sampling period is proportionally reduced. The power consumption of the system versus the F_{OUT} when running at 7GS/s is graphically represented in Fig. 6.23. The complete-DDFS-solution exhibits a maximum power consumption of about 615mW when the RSTC method is enabled. Similarly, the peak dissipation when the RSTC-DEM is disabled reaches 595mW. A penalty of about 20mW in power consumption is paid when activating the dynamic element matching engine. Finally, in Fig. 6.24, the absolute phase noise at F_{OUT} = 926.4MHz was measured when enabling and disabling the RSTC-DEM engine. The single sideband phase noise (SSB) was measured to be around -134dBc/Hz at a 100KHz offset from the carrier.

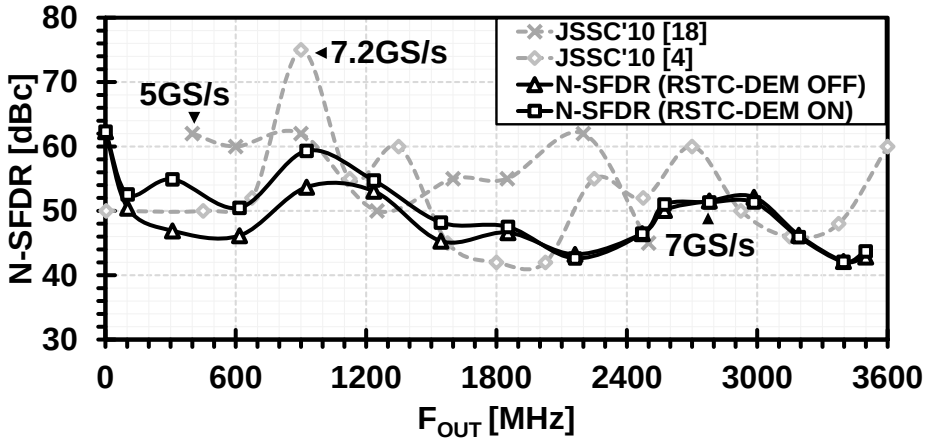


Fig. 6.19. Measured N-SFDR vs DM-DDFS output frequency.

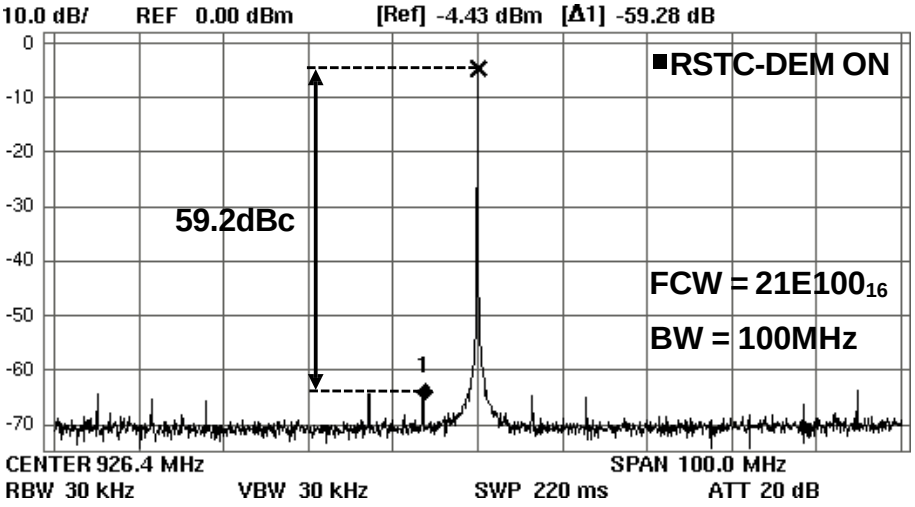


Fig. 6.20. N-SFDR sweet-spot. F_{OUT} = 926.4MHz. *SR* = 7GS/s.

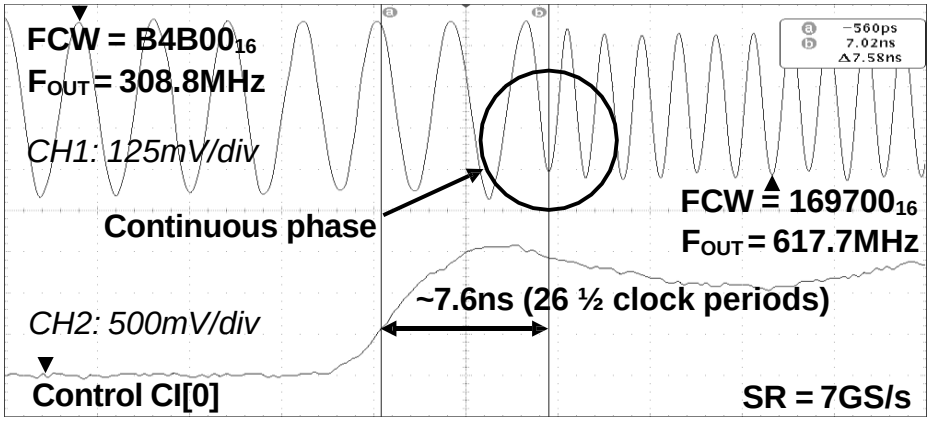


Fig. 6.21. System latency.

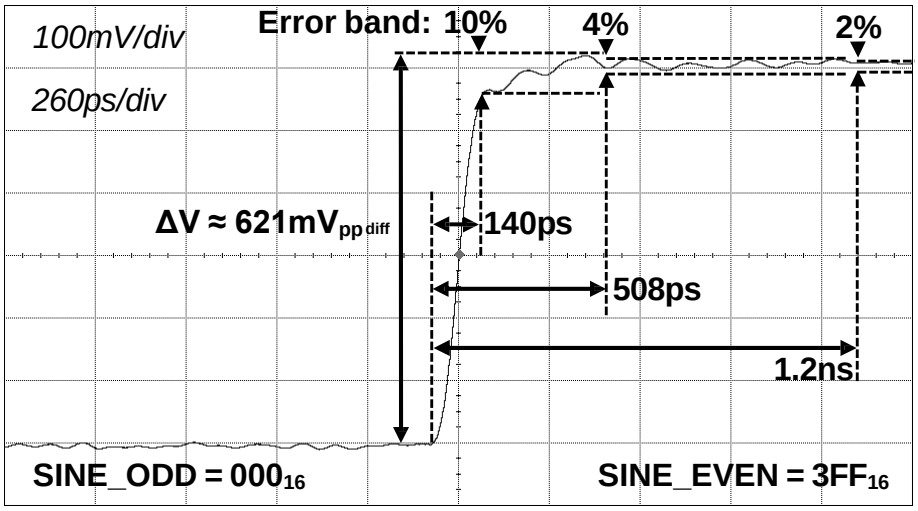


Fig. 6.22. Full-scale settling time.

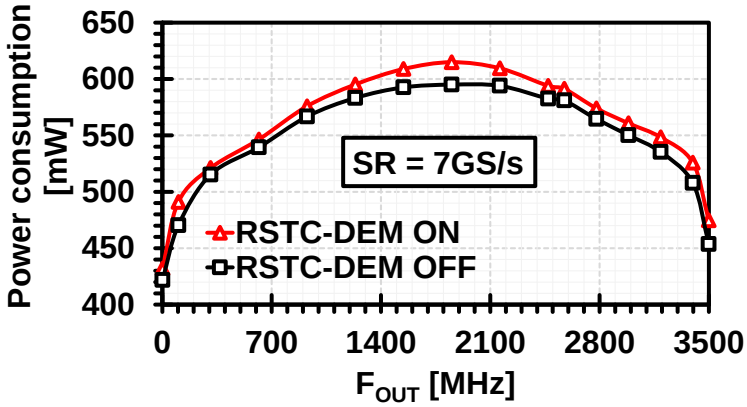


Fig. 6.23. Power consumption vs DM-DDFS output frequency.

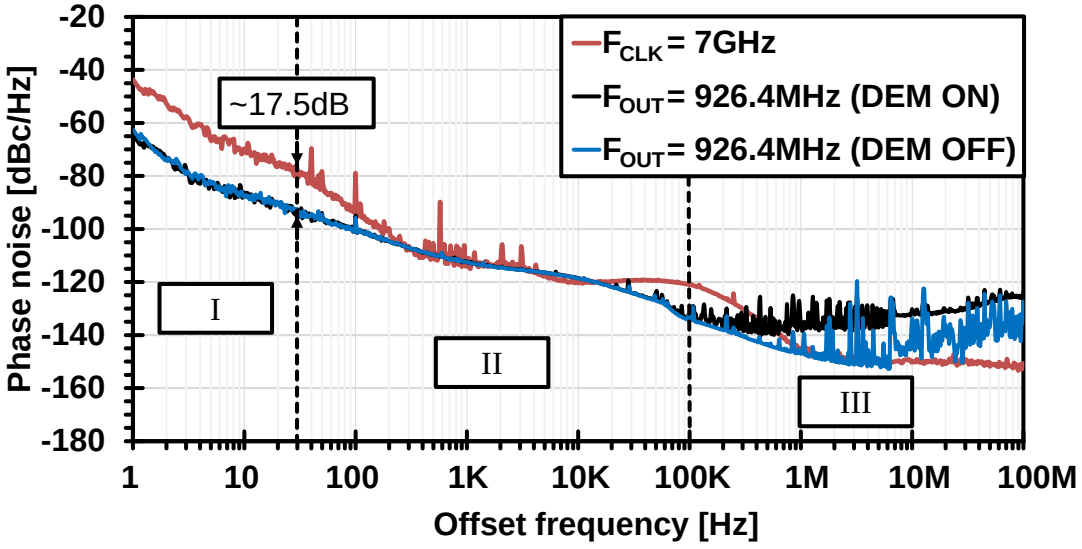


Fig. 6.24. Absolute phase noise at F_{OUT} = 926.4MHz.

As expected, the phase noise characteristics deteriorate when enabling the RSTC-DEM method. However, it should be noticed that it only affects the SSB noise shape at offset frequencies above 100KHz. A reduction in the maximum spur level with a simultaneous increase in the noise floor was observed in this range. Another important outcome of this measurement is that, by enabling and disabling the DEM method, the 2I-RDAC contribution to the absolute phase noise in the output carrier can be clearly observed. The residual phase noise curves are not reported since the system clock was internally generated (internal divider-by-two circuit) and its exact noise contribution is undetermined. However, it should be noticed how the phase noise characteristics reasonably follow the model described in Chapter 1 up to about 30Hz offset from the carrier [14]. As expected, and improvement of about 17.5dB was observed (1.5). In summary, the region I in Fig. 6.24 is clearly dominated by the reference clock noise. On the contrary, the RSTC-DEM method helps to highlight the zone in which the 2I-RDAC contribution is dominant. Although the nature of the noise shape in region II can't be confirmed by measurement with this setup, it is suspected to be determined by the noise contributions of the internal blocks including the clock divider, the clock tree structure and/or the power supply noise.

6.2.3 Performance comparison

This work demonstrates for the first time the operability of a CMOS-based DDFS above 2GS/s. Table 6-3 and Fig. 6.25 respectively lists and represents the state of the art of this technology including this work. The required clock (F_{CLK}) for synthesizing a certain frequency (F_{OUT} in (1.1)) is halved by combining a complementary dual-phase latch-based DM-DDFS core and a two-times interleaved RDAC. A high-speed RSTC-DEM architecture has been also introduced, allowing an N-SFDR gain up to 8dB when operating at 7GS/s with output carriers below 1.85GHz (Fig. 6.17, Fig. 6.19 and Fig. 6.24). The dynamic errors become dominant above that frequency, limiting the N-SFDR to 42dBc. The measured prototypes exhibit spur lines at $SR/2 \pm F_{OUT}$ due to timing errors among the interleaving channels [54] (Fig. 6.15). The worst case W-SFDR was 32dBc. It should be noted that similar to [4], [18] and unlike [6], [7], [9], [19], all the measurements were carried out by employing packaged prototypes. The proposed RDAC draws a code-dependent current from the power supply that, combined with the parasitics in the interconnections and bonding wires, generates non-linear distortions. The performance of the integrated 2I-RDAC can be also compared with recently published RF-DACs (Table 6-4). It should be noticed that the distinctive feature of the described 2I-RDAC resides in its ability to achieve a rail-to-rail operation.

TABLE 6-3: PERFORMANCE COMPARISON

DDFS Metrics	This Work		JSSC'10 [18]	JSSC'10 [4]	JSSC'11 [6]	JSSC'06 [7]	MWCL'08 [19]	JSSC'14 [9]
	DEM ON	DEM OFF						
Architecture	DM		NLD(1)	NLD	AM	NLD	DM	NLD
Technology	65nm CMOS		0.13µm SiGe	0.13µm SiGe	0.35µm SiGe	InP DHBT	InP DHBT	55nm CMOS
Freq./Amp. Resol. [bits]	24/10		24/10	11/10	9/8	8/5	12/7.5	32/9
W-SFDR [dBc]	32(1)		38(1) (2)	33(1) (3)	45.7(4)	21.6(5)	30.7(5)	55.1(4)
N-SFDR [dBc]	42(1)		45(1)	42(1) (3)	-	-	-	-
Area [mm²]	0.22/1.3(6)		7.5/11.1(6)	7.5/14(6)	2.1(6)	3.9(6)	16.5(6)	0.1/0.3(6)
SR [GS/s]	7		5	8.6	5	32	24	2
Power [mW]	615	595	4700	4800	460	9450	19800	130
FoM(7)	458.9	474.3	85.8	81.1	2133.3	41.1	42.1	8944.3
PE [mW/(GS/s)]	87.9	85	940	558.1	92	295.3	825	65

(1) *Packaged/test board.* (2) *Best case.* (3) *@ 7.2GS/s.* (4) *Die-on-board.* (5) *On-wafer probed.*

(6) *Including pads.* (7) $FoM = \frac{2^{W - SFDR[dBc]/6} \cdot SR[GS/s]}{Power[W]}$ *[9]*

TABLE 6-4: PERFORMANCE COMPARISON WITH RECENTLY PUBLISHED RF-DACS

Reference	This Work	A-SSCC'13 [74]	JSSC'15 [54]	ISSCC'17 [32]
Architecture	Interleaved Shared R No duty-cycle calibration	Interleaved Delay-line duty-cycle calibration	Interleaved Back-gate duty-cycle calibration	Dual-Mode RF-DAC No interleaving
Technology	65nm CMOS	65nm CMOS	28nm FDSOI	16nm FinFET
Resolution [bits]	10	12	9	14
SR [GS/s]	7	1.7	11	6.8
Worst case W-SFDR [dBc]	32	58	52	62
Active area [mm²]	0.11	0.4	0.04	0.855
V_{SUPPLY} [V]	1.2	1.2	1.0	0.85/0.72
Power [mW]	~312(1)	70	110	330
Swing [$V_{pp\text{-}diff}$]	1.2	0.5	0.425	-

(1) *LPE simulation.*

It should be noticed that this work achieves a 7GS/s throughput with a rail-to-rail operation in CMOS technology without using any duty-cycle calibration technique. This is a distinctive feature which is difficult to achieve in current-steering based converters. Finally, a trade-off between the N-SFDR and the signal-to-noise ratio (SNR) arises when enabling the RSTC-DEM mechanism (Fig. 6.17 and Fig. 6.24). To the extent of our knowledge, the highest sampling rate was reported in [7] and the fastest DM-DDFS was described in [19].

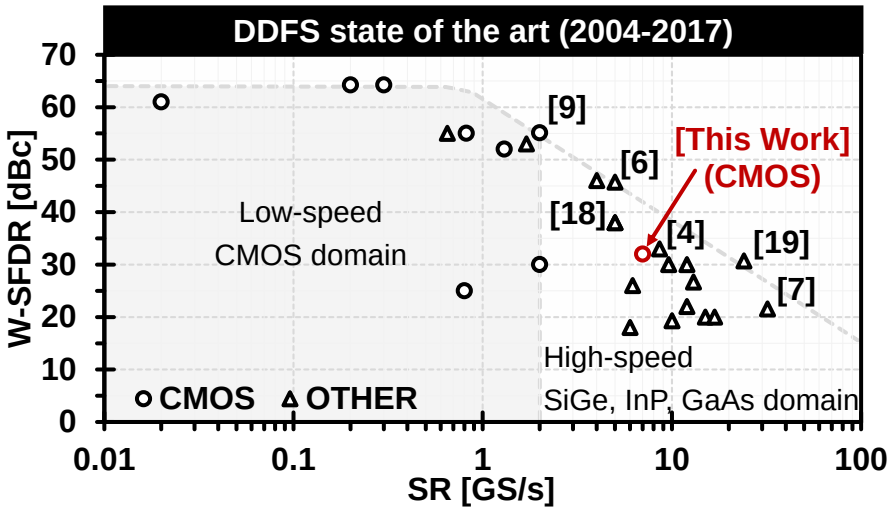


Fig. 6.25. W-SFDR vs. sampling rate.

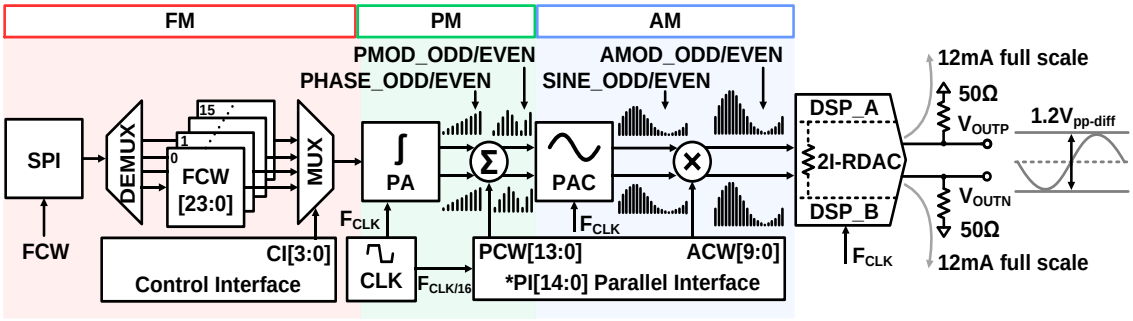
The best timing performance among CMOS-based DDFSs and finest FoM were disclosed in [9]. This CMOS implementation not only achieves a 7GS/s operation with a frequency resolution of 417.2Hz but also outperforms in terms of power efficiency when compared to [4], [6], [7], [18], [19]. Additionally, it exhibits the smallest area when contrasting with DDFSs based on compound semiconductors [4], [6], [7], [18], [19] while equaling the best accumulator size and amplitude resolution among them [18]. The third best FoM in Table 6-3 was achieved as well.

6.2.2 Summary of a 7GS/s DDFS with a two-times interleaved RDAC in 65nm CMOS

Relevant aspects related to the evaluation of the first complete-DDFS-solution running at 7GS/s in CMOS technology have been presented in this section. With the smallest active area among designs above 2GS/s, the proposed system only consumes 87.9mW/(GS/s) from a 1.2V power supply when the RSTC-DEM method is enabled. This flexible architecture can be digitally configured and adapted to the requirements of different wireless standards, waveforms, frequency bands, and operation modes. Such performance paves the way for new DDFS applications including but not limited to frequency exploration, software defined radio (SDR) and SoC transceivers. By integrating a two-times interleaved RDAC, an amplitude swing of $1.2V_{pp\text{-}diff}$ can be achieved in 65nm CMOS. Moreover, this is a digitally-intensive RFIC solution and potential benefits in terms of delays and energy efficiency are expected when moving to more advanced CMOS technology processes [10]. Sampling frequencies above 10GS/s could be potentially achieved when implementing the proposed architecture in CMOS processes having smaller channel lengths.

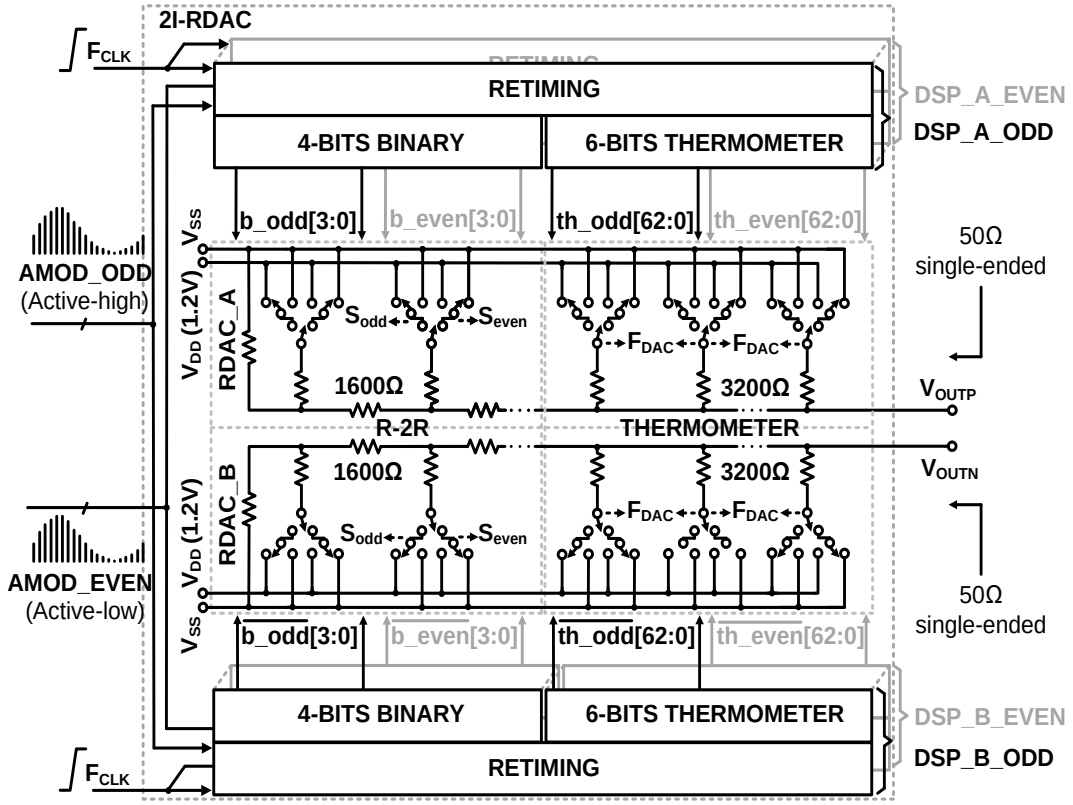
6.3 A High-speed DDFS MMIC with frequency, phase and amplitude modulations in 65nm CMOS technology

Finally, the third prototype demonstrates a high-speed complete-DDFS solution with FM, PM and AM capabilities (Fig. 6.26 and Fig. 6.27). This digitally intensive architecture constitutes the first DM-DDFS reported at 7GS/s and including all the modulation functionalities.



*PI[14] = 0 → PI[13:0] = PCW, PI[14] = 1 → PI[9:0] = ACW

Fig. 6.26. 7GS/s complete-DDFS-solution featuring FM, PM and AM capabilities.



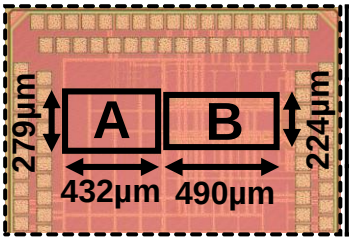
F_{CLK}: System clock F_{DAC}: Interleaving clock (skewed version of F_{CLK})

Fig. 6.27. Simplified two-times interleaved RDAC.

High-speed solutions for every component of the DDFS architecture are implemented and evaluated. The throughput can be increased when compared with previous arts by employing a fully pipelining architecture that can output two samples per clock cycle. The complementary dual-phase latch-base synchronization method is employed in every digital block. A simplified version of the 2I-RDAC is used this time. No DEM functionality is implemented since it has been observed that the dynamic effects are dominant at high sampling rates. Hence, a more compact and simple converter will be beneficial in terms of area and power efficiency (Fig. 6.27).

6.3.1 Implementation

A proof-of-concept chip was fabricated in a 1P9M 65nm CMOS process (Fig. 6.28). All the digital logic was designed by using standard-cell technology and a fully synthesizable flow. The total die area is 0.98×1.46mm^2. The prototypes were also encapsulated in LQFP packages and assembled in an evaluation board made of FR-4. The reference clock is driven by an Agilent E8257D signal generator. An MS2830A signal analyzer from Anritsu, an Agilent DSO90804A high-performance oscilloscope and an E5052B Signal Source Analyzer from Keysight were also employed. A KCU105 FPGA board from Xilinx was used in order to implement the system controller and the digital baseband processing.



REFERENCE	CORE	AREA
A	NCO FM+PM+AM	0.12mm^2
B	2I-RDAC	0.11mm^2

Fig. 6.28. Die micrograph. 7GS/s + FM/PM/AM DM-DDFS solution.

6.3.2 Device characterization

The N-SFDR (bandwidth ≈ 1.4% of the *SR*) and time domain measurements of a 926.4MHz synthesized carrier are reported in Fig. 6.29. This system can switch between different output frequencies with a latency of about 12.86ns (45 clock periods at 7GS/s) (Fig. 6.30). The increased latency results from the insertion of the pipelined phase-adder and the amplitude-modulator in the NCO core.

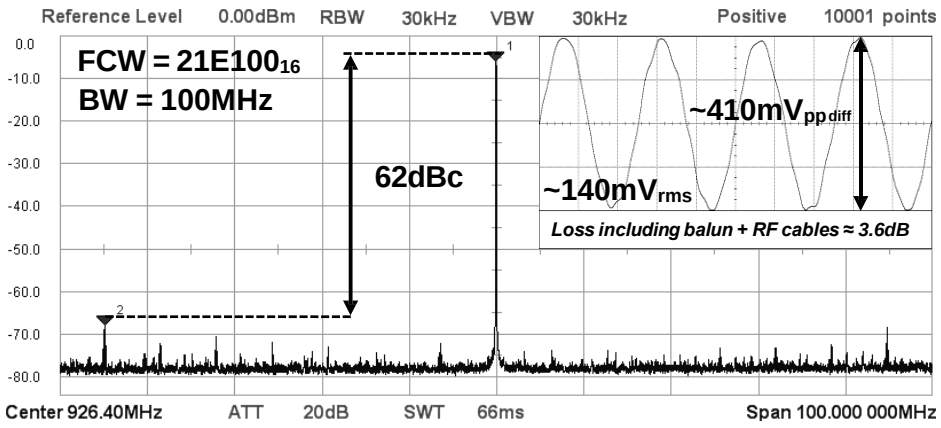


Fig. 6.29. N-SFDR at F_{OUT} = 926.4MHz. *SR* = 7GS/s.

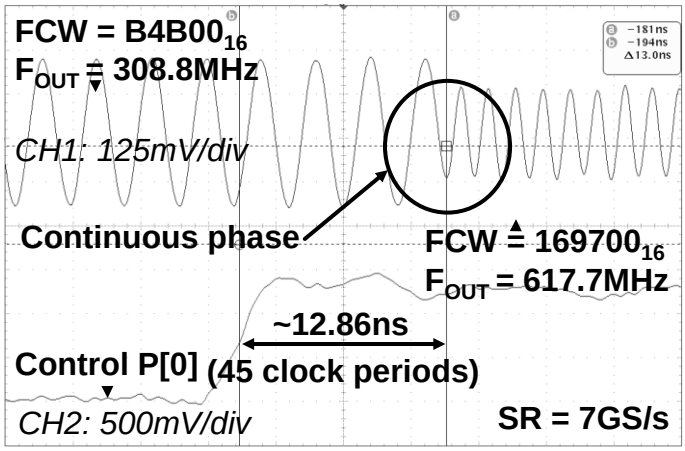


Fig. 6.30. System latency.

6.3.2.1 Linear frequency modulation

The linear frequency modulation (LFM) method has been employed in surveillance radar operating in the frequency range of 2.7GHz-2.9GHz with a typical necessary bandwidth (B_N) of 6MHz [75]. Out-of-band (OoB) masks have been defined in order to evaluate the spectrum emissions [75]. Fig. 6.31 graphically represents the measured spectrum of a synthesized LFM pulse signal with a 2.6MHz frequency deviation (B_c) [75]. It can be observed that the achieved performance satisfies the mask requirement for a -40dB bandwidth (B_{-40dB}) of 14MHz (calculated from [75]). Equations (6.1) to (6.4) can be used to determine the B_{-40dB} bandwidth according to the length of the compression pulse and its rise and falling time characteristics [75]. The necessary bandwidth can be estimated according to (6.5). Fig. 6.32 represents a wide-band frequency sweep among 7 pre-stored *FCW* registers generated by driving the 4-bit

control interface with a digital ramp. The signal level reduction results from uncompensated losses including the interconnection and cables attenuation.

$$B_{-40dB} = 1.5\left\{B_C + \sqrt{\pi}\cdot\left[\ln\left(B_C\cdot\tau\right)\right]^{0.53}\cdot\left[Min\left(B_{rise}, B_{fall}, B_{rise\&\,fall}\right) + Max\left(B_{rise}, B_{fall}, B_{rise\&\,fall}\right)\right]\right\} \quad (6.1)$$

Where:

$$B_{rise} = \frac{1}{\sqrt{\tau\cdot t_r}} \quad (6.2)$$

$$B_{fall} = \frac{1}{\sqrt{\tau\cdot t_f}} \quad (6.3)$$

$$B_{rise-fall} = \frac{1}{\sqrt[3]{\tau\cdot t_r\cdot t_f}} \quad (6.4)$$

$$B_N = \frac{1.79}{\sqrt{\tau\cdot t_r}} + 2B_C \quad (6.5)$$

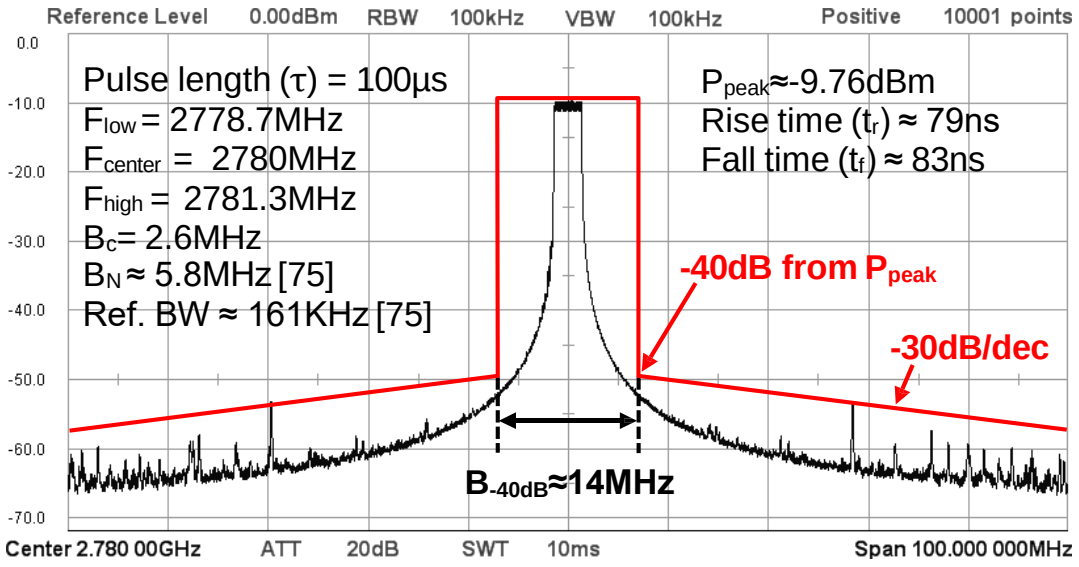


Fig. 6.31. LFM spectrum and OoB mask. *SR* = 7GS/s.

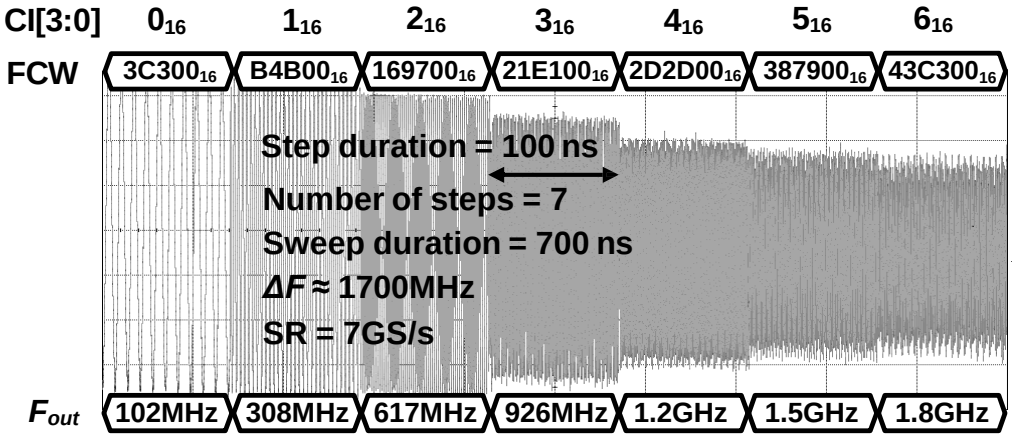


Fig. 6.32. Wide-band frequency sweep among 7 pre-stored *FCW* registers.

6.3.2.2 Binary phase shift keying and on-off keying

Binary phase shift keying (BPSK) and on-off keying (OOK) baseband signals have been employed to modulate the DDFS output carrier and demonstrate the PM and AM capabilities. Fig. 6.33 and Fig. 6.34 represent the measured time domain and the frequency spectrum of a BPSK and OOK modulated carrier. Gaussian pulse-shaped spectrums are also reported for better completeness. The measured transition from 0° to 180° of a 926.4MHz BPSK modulated carrier is also shown in Fig. 6.33. In Fig. 6.34, rectangular and Gaussian pulse-shaped OOK modulated carriers with equivalent binary sequences can be observed. The information source is a 16-bits PRBS generator. It should be noted that the throughput bottleneck of this system is the general purpose interface (PMOD-GPIO) used as the output from the FPGA board (20Mbps) [76].

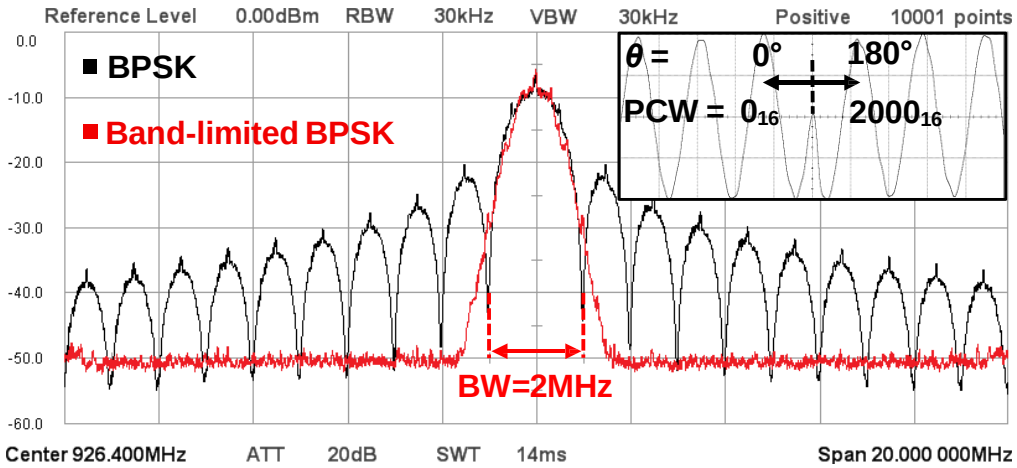


Fig. 6.33. 1Mbps BPSK modulated signal. Spectra and time domain waveform. $F_{carrier}$ = 926.4MHz. *SR* = 7GS/s.

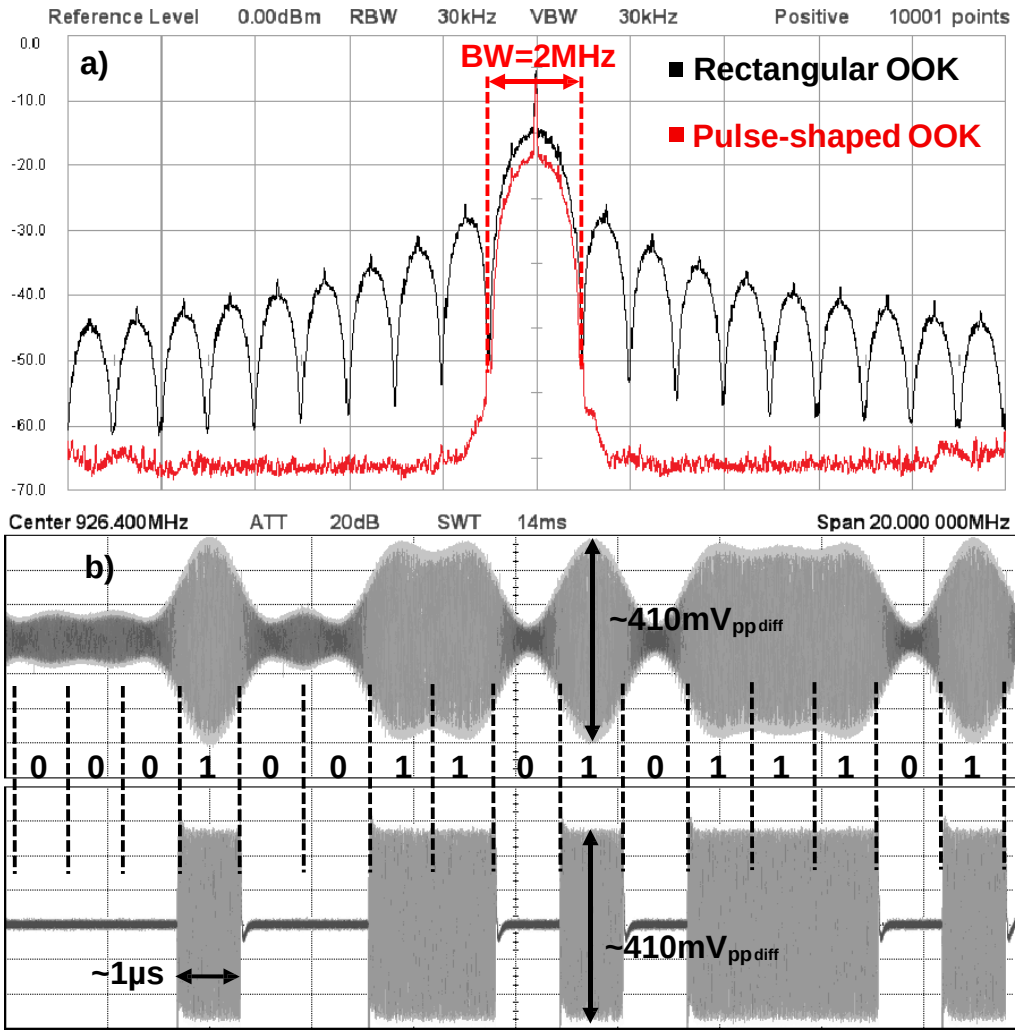


Fig. 6.34. 1Mbps OOK modulated signal. Spectra (a) and waveforms (b) with and without Gaussian pulse-shaping. $F_{carrier}$ = 926.4MHz. SR = 7GS/s.

The maximum bitrate is limited to 1Mbps when setting an oversampling ratio (OSR) of 20 in the baseband processing unit. Higher bitrates could be possible if implementing a high-speed serial interface (SERDES) in both the off-chip baseband unit and the DDFS input interface.

6.3.3 Phase noise

As previously discussed in Chapter 1, the phase noise in a DDFS system is reduced according to the ratio between the system clock and the output carrier frequency. The phase noise performance will improve according to (1.5) [13]. The absolute SSB phase noise is represented and contrasted at different frequencies in Fig. 6.35.

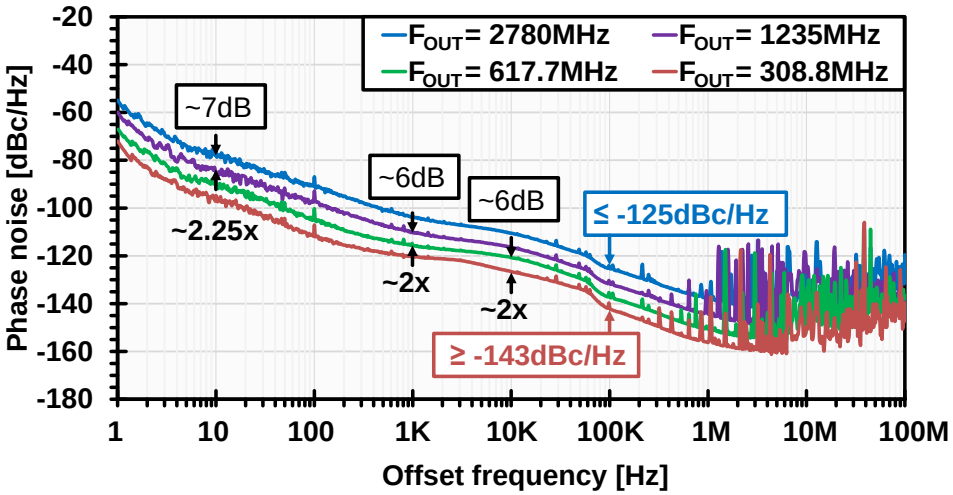


Fig. 6.35. Measured absolute phase noise.

The SSB phase noise was measured to be around -77.8dBc/Hz at 10Hz offset from the carrier when F_{OUT} = 2780MHz. The measured value was -85dBc/Hz when lowering the output frequency to about 1235MHz and at the same deviation from the fundamental. This represents an improvement of nearly 7.2dB (Fig. 6.35). The measured results confirm the model estimations of 7.04dB when reducing the output frequency from 2780MHz to 1235MHz (1.5). Similarly, about 6dB improvements were observed when changing the output frequency to F_{OUT} = 617.7MHz and 308.8MHz at 1KHz and 10KHz away from the carrier respectively. It should be noticed that the frequency ratios among the last three synthesized frequencies are roughly 2. Hence, the 6dB improvement matches the model projections. The spur contents resulting from the phase truncation and the correlated quantization errors mechanisms can be also observed [15]. The absolute single sideband phase noise at 100KHz offset was better than -125 dBc/Hz in all the evaluated frequencies. It reaches nearly -143dBc/Hz when F_{OUT} = 308.8MHz at a 100KHz offset from the carrier.

6.3.4 Energy performance

The curves in Fig. 6.36 represents the measured power consumption when employing a 1.2V digital (*DVDD*) and analog (*AVDD*) voltage sources. Since this is a digitally intensive architecture, the total energy consumption is highly dependent on the switching activity. The dynamic consumption increases proportionally with the sampling rate. It also differs between *FCW*s when keeping a constant frequency in the clock signal. The sampling rate was changed in 500MS/s steps up to the maximum throughput of 7GS/s in Fig. 6.36. The power consumption was measured at these discrete steps under four different *FCW* settings (*FCW1*, *FCW4*, *FCW7* and *FCW11* in

Table 5-1). The maximum value was registered at 7GS/s when the *FCW7* value in Table 5-1 was configured (601mW divided into 529.56mW dissipated by the digital logic and 71.44mW consumed by the analog section).

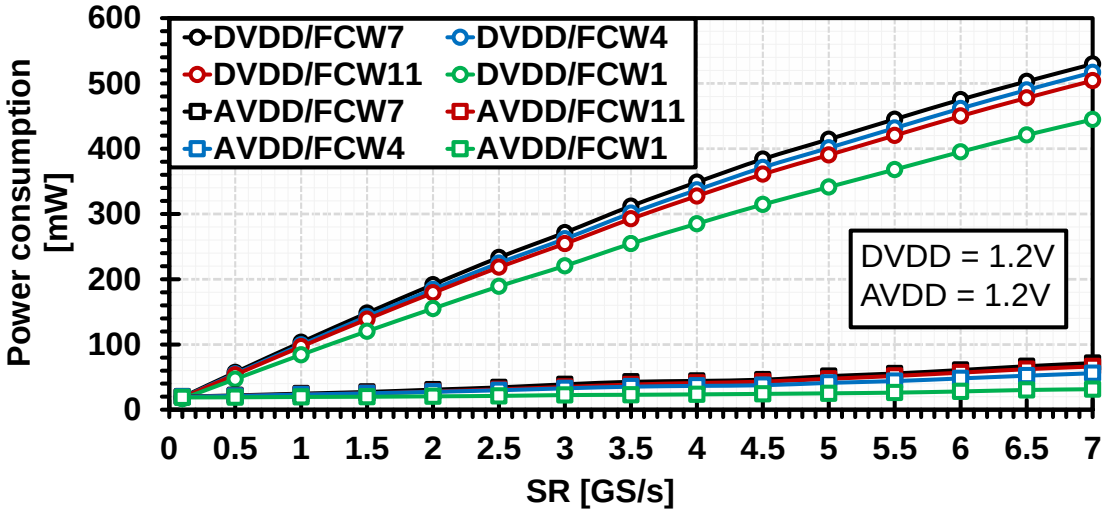


Fig. 6.36. Power consumption vs. sampling rate.

6.3.5 Summary of a high-speed DDFS MMIC with frequency, phase and amplitude Modulations in 65nm CMOS

This study demonstrates for the first time the frequency, phase and amplitude digital modulation capabilities of a CMOS-based DDFS when running at 7GS/s (Table 6-5).

TABLE 6-5: PERFORMANCE COMPARISON

DDFS Metrics	This Work	JSSC'10 [18]	IMS'09 [77]	JSSC'11 [6]	T-MTT'10 [36]
Architecture	DM-DDFS	NLD-DDFS	NLD-DDFS	AM-DDFS	AM-DDFS
Technology	65nm CMOS	0.13µm SiGe	0.13µm SiGe	0.35µm SiGe	0.35µm SiGe
Freq./Amp. Resol. [bits]	24/10	24/10	9/7	9/8	8/6
W-SFDR [dBc] (1)	32(1)	38(1) (2)	-	45.7(3)	20(3)
N-SFDR [dBc]	42(1)	45(1)	35(1)	-	-
Area [mm²]	0.23/1.43(4)	7.5/11.1(4)	3.4/7.5(4)	2.1(4)	1.15(4)
SR [GS/s]	7	5	2.9	5	16.8
Power [mW]	601	4700	2000	460	486
FoM(5)	469.6	85.8	-	2133.3	348.4
PE [mW/(GS/s)]	85.9	940	689.6	92	28.9
FM/PM/AM	Yes/Yes/Yes	Yes/Yes/No	Yes/Yes/No	Yes/No/No	Yes/No/No

(1) *Packaged/test board.* (2) *Best case.* (3) *Die-on-board.* (4) *Including pads.*

(5) $FoM = \frac{2^{W-SFDR[dBc]/6} \cdot SR[GS/s]}{Power[W]}$ *[9]*

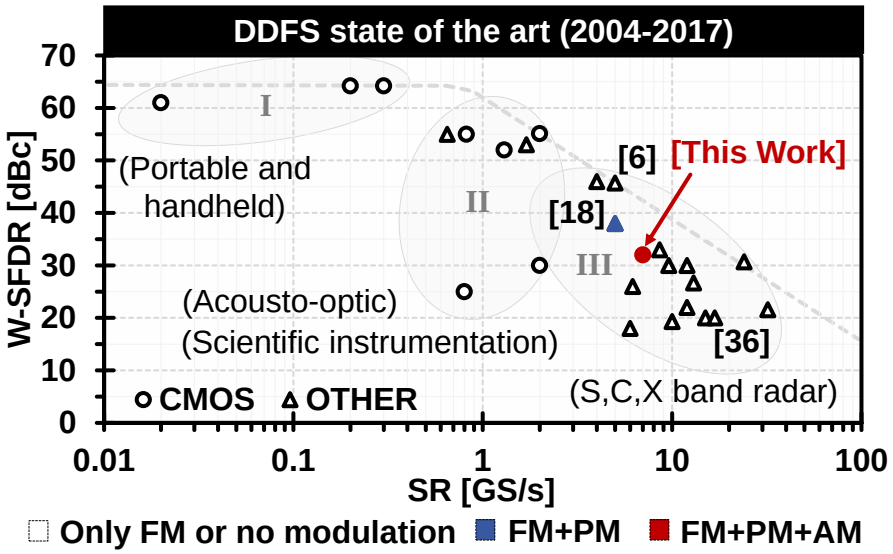


Fig. 6.37. W-SFDR vs. sampling rate.

To the best of our knowledge, the only references supporting at least frequency and phase modulation and operating in excess of 2GS/s are [18] and [77]. Compared to these previous works, the proposed architecture not only achieves a higher sampling rate while equaling the best frequency and amplitude resolutions [18] but also attains superior area, power efficiency and FoM metrics as reported in Table 6-5 and Fig. 6.37. Moreover, this design employs a CMOS technology instead of the more costly SiGe alternative, paving the way for new DDFS applications including but not limited to frequency exploration, polar modulation, and SDR.

6.4 Summary of the proof-of-concept chips

In this chapter three complete-DDFS-solutions implemented in 65nm CMOS technology has been described. Each of them exhibits unique features as listed in Table 6-6. In summary, the merits of the proposed design methodology aimed to maximize the throughput in CMOS-based DDFSs has been demonstrated with practical designs. Solutions for all the blocks in the DM-DDFS architecture has been implemented and evaluated. Additionally, the RSTC-DEM has been applied in the direct digital synthesis technique for the first time. The measured results show a gain up to 8dB in the N-SFDR when using this method. These results highlight the potentials of the CMOS technology for being employed in digitally intensive frequency generation techniques aiming higher throughputs and lower power consumption.

TABLE 6-6: MAIN FEATURES OF THE IMPLEMENTED COMPLETE-DDFS-SOLUTIONS

Complete-DDFS-Solution	**2GS/s DM-DDFS [47]**	**7GS/s DM-DDFS [48]**		**7GS/s-FM+PM+AM DM-DDFS [49]**
		DEM ON	**DEM OFF**	
Architecture	DM-DDFS	DM-DDFS		DM-DDFS
Technology	65nm CMOS	65nm CMOS		65nm CMOS
Freq./Amp. Resol. [bits]	24/10	24/10		24/10
W-SFDR [dBc]	30(1)	32(1)		32(1)
N-SFDR [dBc]	-	42(1)		42(1)
Area [mm²]	0.142/1.25(2)	0.22/1.3(2)		0.23/1.43(2)
SR [GS/s]	2	**7**		7
Power [mW]	118	615	595	601
FoM (3)	542	458.9	474.3	469.6
PE [mW/(GS/s)]	**59**	87.9	85	85.9
FM/PM/AM	Yes/No/No	Yes/No/No		**Yes/Yes/Yes**
Feature	**Best PE among CMOS-based DDFSs**	**Fastest CMOS-based DDFS**		**First DDFS operating at 7GS/s with FM+PM+AM**

(1) *Packaged/test board.* (2) *Including pads.* (3) $FoM = \frac{2^{W-SFDR[dBc]/6} \cdot SR[GS/s]}{Power[W]}$ *[9]*

CHAPTER 7:
CONCLUSIONS AND FUTURE WORK

THIS dissertation has been focused on the study of techniques aimed to maximize the throughput in CMOS-based DDFSs. The proposed methodology deviates from the conventional methods employed up to date in high-speed DDFS applications. Instead of relying on analog-centric architectures [4] [6], the increase of the speed in a CMOS-based DM-DDFS was achieved by reducing the complexity of the analog sections and employing digital optimization/compensation techniques. The outcomes of this work could be of relevance both for the academy and for the industry. Although specific applications have been targeted, the same design methodology can be employed in other digitally intensive architectures requiring higher performance or better energy efficiency. Three functional prototypes have been evaluated in 65nm CMOS technology. Each of them demonstrates different features of the proposed solutions. A summary of the techniques and results presented in this dissertation is given in the following sections.

7.1 Academic perspective

Several methods intended to increase the throughput in every block of the DM-DDFS architecture are described in this study. In the digital phase domain, a 24-bits complementary dual-phase latch-based phase accumulator (C2P-PA) that can generate two complementary samples per clock cycle was implemented. This circuit is characterized in terms of timing and energy performance. Equations for the estimation of the equivalent occupied area are provided in this work. Also, a dual-phase sum of product terms based phase to amplitude converter (SoP-PAC) that can match the speed of the digital phase domain block by using a feed-forward topology is discussed in detail. These two techniques enable for the first time the operation of an NCO core at 7GS/s in CMOS technology. Since this kind of numerically controlled oscillator is a component commonly found in mixed-signal systems such as radar, digital PLLs and optical drivers, the described approach could be of interest in future investigations.

A two-times interleaved RDAC achieving a rail-to-rail operation with a code independent output impedance was presented in the analog domain. The circuit operation is discussed, including a high-speed architecture for the RSTC-DEM method. More importantly, the benefits and drawbacks of this RDAC architecture are associated with the circuit structures and the models employed during the system simulation. All these materials could be of relevance in studies related to high-speed data converters and interleaving architectures. Furthermore, the digital structures that enable the frequency, phase and amplitude modulation capabilities in the NCO core were investigated. Relevant design equations are described and post-layout simulation results are compared with conventional approaches. Table 7-1 relates the main techniques composing the proposed design approach.

TABLE 7-1: SUMMARY OF THE TECHNIQUES COMPOSING THE PROPOSED DESIGN APPROACH

Domain	Digital phase	Digital amplitude	Analog
Proposed design methodology for high-speed CMOS-based DM-DDFS solutions	● Pipelined accumulator and phase-adder ● Complementary dual-phase latch-based sequencing method	● Sum of product terms based PAC ● Parallel multiplier ● High-speed RSTC-DEM ● Complementary dual-phase latch-based sequencing method ● Pipelining	● RDAC ● Two-times interleaving ● Common resistor array between complementary DSP units ● Hybrid clock distribution network

Instead of employing analog-centric architectures such as NLD-DDFS or AM-DDFS, a digitally intensive DM-DDFS with an RDAC core is proposed. Previous high-speed synthesizers [4], [6], [7], rely on replacing the PAC block by some sort of analog converter. However, this approach tends to increase the complexity of the analog sections and employs current mode logic (CML) instead of CMOS logic [4]. As a result, the integration density benefits of the advanced CMOS technologies cannot be fully exploited. Interleaving and partial RTC-DEM techniques could be employed in a NLD-DDFS. However, the increased complexity and area of the digital logic makes them impractical solutions. Moreover, synthesizable flows become more difficult since a custom design of the digital and analog blocks is commonly required. These architectures has been mostly implemented in compound semiconductor technologies such as SiGe and InP [4], [6], [7] ([9] reports the fastest CMOS implementation). The proposed approach relies on a digitally intensive architecture that can be implemented by using standard-cell technology (static logic) in a synthesizable flow including

automatic place and route. The analog sections are limited to simple and regular RDAC cells that demands relatively small design and engineering time. The design concept intended to increase the throughput in CMOS-based DDFS is represented in Fig. 7. 1.

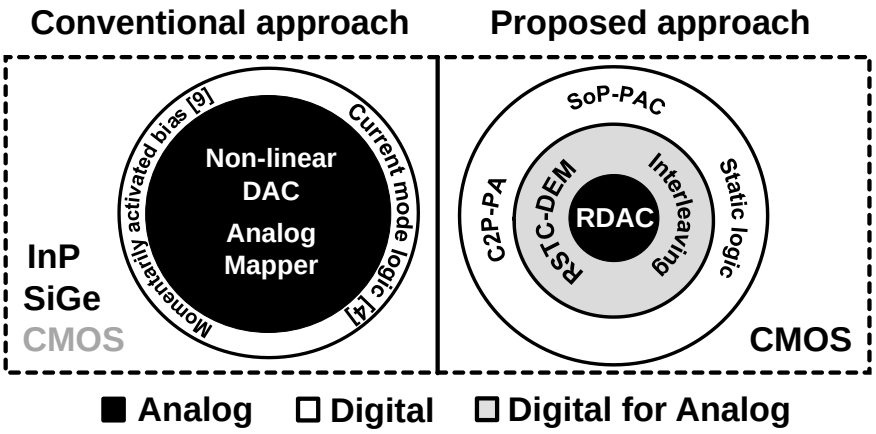


Fig. 7.1. Conventional and proposed design approach for high-speed complete-DDFS-solutions in CMOS technology.

7.2 Industrial perspective

Although this work underperforms in terms of W-SFDR when compared with the commercially available compete-DDFS-solutions, it benchmarks favorably in terms of timing performance and power efficiency. The throughput is increased by 14.3% when compared with the fastest chip in Fig. 7.2. The performance gain reaches 50% when compared with the fastest solution also supporting FM+PM+AM.

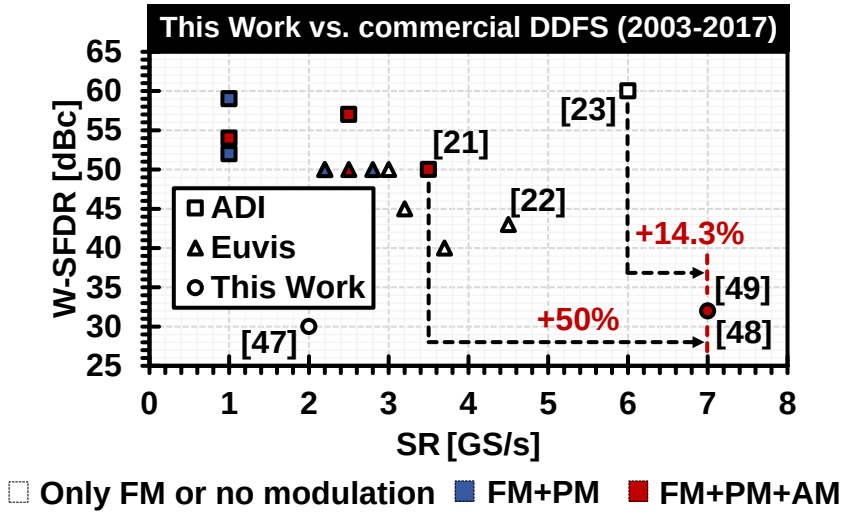


Fig. 7.2. Comparison with commercially available complete-DDFS-solutions. W-SFDR vs. sampling rate.

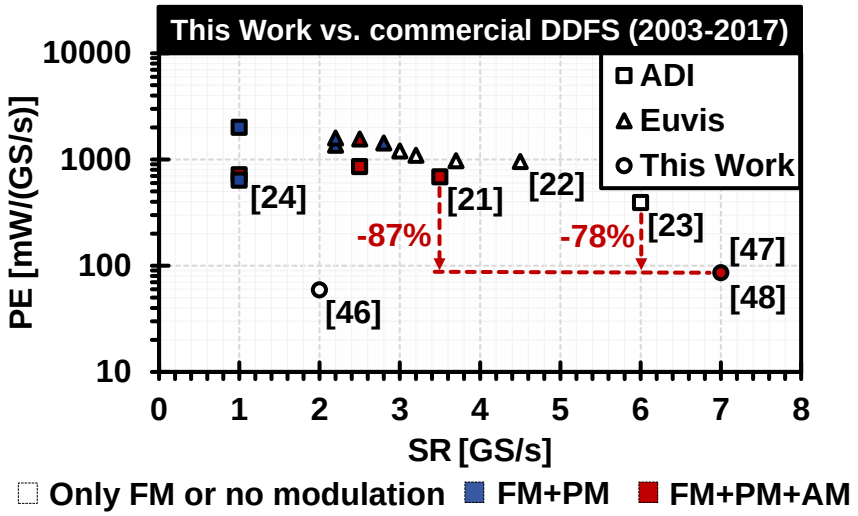


Fig. 7.3. Comparison with commercially available complete-DDFS-solutions. Power efficiency vs. sampling rate.

As can be observed in Fig. 7.3, the power efficiency is also considerably superior. The energy savings exceed 87% when compared with the more efficient commercial DDFS supporting at least FM+PM [24] and nearly 78% contrasted with the fastest commercial chip [23]. All the measurement results are reported by using prototypes encapsulated in LQFP-144 packages and assembled in evaluation boards made of FR-4 substrate. The achieved performance could be of the interest in the industrial sector giving the fact that, under these conditions, superior timing performance and power efficiency has been achieved when compared with commercial devices.

7.3 Application-specific perspective

Two potential applications of the DDFS technology were described in Chapter 1 (radar sensor in SAA systems and a multi-band multi-standard polar modulator). The main requirements were summarized in Table 1-2 and now are contrasted with the achieved performance in Table 7-2. For the first time, this design reports FM+PM+AM modulation capabilities in the digital domain while running at 7GS/s.

TABLE 7-2: TARGET VS. ACHIEVED DDFS PERFORMANCE

Performance	**Technology**	**SR [GS/s]**	**Modulations**			**Power consumption [W]**	**SFDR [dBc]**	
			FM	**PM**	**AM**			
Target	CMOS	≥ 6.8	Yes	Yes	Yes	≤ 1	≥ 43	
Achieved [49]	65nm CMOS	7	Yes	Yes	Yes	≤ 0.601	W-SFDR ≥ 32	N-SFDR ≥ 42

These features enable applications in continuous wave and pulsed radar sensors as well as in polar modulators systems. It can be observed how the achieved performance exceeded the target sampling rate of 6.8GS/s. This operation allows to directly cover all the broadcasting standards up to 2.7GHz and SAA applications allocated in the S-band (2.4GHz) [39]. The coverage can be extended to higher frequencies by employing analog multipliers together with the implemented complete-DDFS-solutions. Furthermore, the DDFS reference can be driven by a low phase noise dielectric resonator oscillator, resulting in a feed-forward, PLL free, architecture [36]. The worst case power consumption when running at maximum sampling rate was 601mW [49]. This represents a considerable improvement in terms of energy efficiency when compared with commercial devices [23] [24] and previously reported high-speed synthesizers [7] [18]. Reducing the power consumption of the synthesizer core is a critical factor when integrating the DDFS solutions on onboard SAA solutions due to the often limited power budget. Although the W-SFDR (≥32dBc) does not satisfy the original target (≥43dBc), the N-SFDR is often considered of greater significance since wideband spurs can be relatively easily filtered [4]. The N-SFDR performance (RSTC-DEM OFF) is compared with the SFDR requirement of different broadcasting standards in Fig. 7.4. It can be observed how the implemented high-speed complete-DDFS-solutions [48] [49], satisfies the requirements of the different broadcasting and frequency exploration systems represented in Fig. 7.4 (except at F_{OUT} ≈ 2160MHz were it falls 1dB below the 43dBc limit [46]). In all cases, the N-SFDR was measured within 100MHz. This bandwidth can typically support the requirements of the different standards listed in Fig. 7.4 [78]-[80]. The worst conditions can occur in applications employing Digital Video Broadcasting - Satellite - Second Generation Extensions (DVB-S2X) with wideband transponders exceeding 100MHz [78]. The absolute SSB phase noise at a 100KHz offset from the carrier was better than -125 dBc/Hz in all the evaluated frequencies below 2.8GHz.

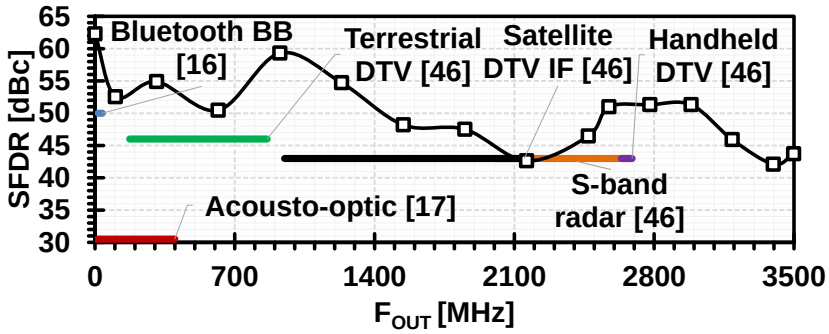


Fig. 7.4. Measured N-SFDR performance vs. required SFDR.

7.4 Future work

Future efforts should be concentrated in four main topics: enhancements in the dynamic performance, further reduction of the energy consumption, increase of the throughput and fully-synthesizable architectures. This dissertation already covers some of these areas but there is still a margin for improvements that can be exploited. Fig. 7.5 graphically represents these ideas by showing the progress history of this work as well as the future target area. Since the proposed design methodology results in a digitally intensive architecture, improvements are expected when moving to more advanced CMOS technologies. The last report from International Technology Roadmap for Semiconductors (ITRS) released in 2015 predicts the physical gate length (L_{gate}) reduction going flat in the upcoming years (Fig. 7.6) [81].

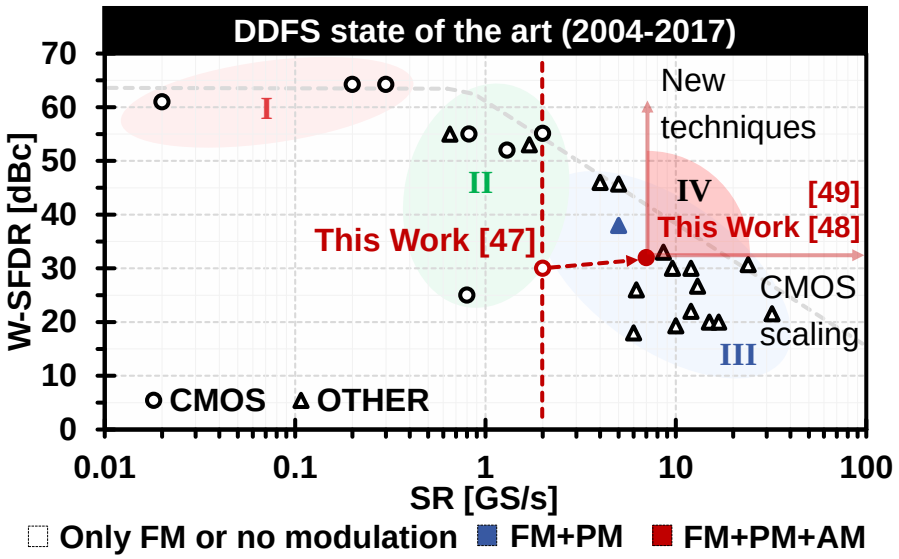


Fig. 7.5. Progress history of this work and target area.

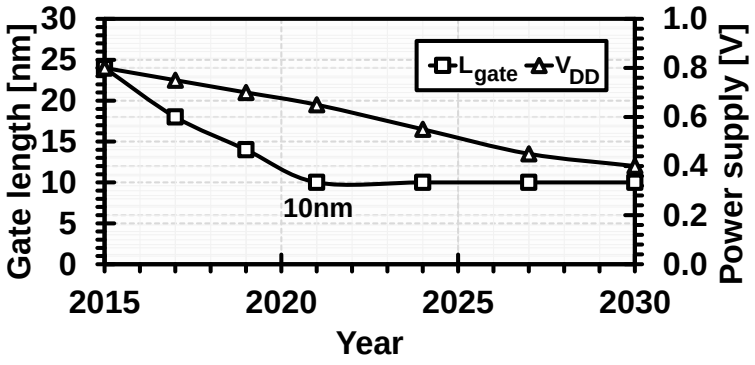


Fig. 7.6. 2015 ITRS logic core device technology roadmap. Physical gate length (L_{gate}) and power supply voltage (V_{DD}).

Besides, the power supply voltage is expected to continue scaling down to 0.4V (Fig. 7.6) [81]. As a result, reductions in the energy per switching are also expected (Fig. 7.7) [81]. Although the current technology trends appears to be more focused on reducing the power consumption rather than increasing the performance, the intrinsic delay of the high-performance transistors is expected to continue decreasing by a factor of 4× (Fig. 7.7) [81]. Interleaving DACs operating up to 11GS/s has been already reported in 28nm FDSOI CMOS technology [54]. Table 7.3 summarizes the most important benefits and drawbacks that could arise from the adoption of more advance CMOS technology process. The proposed complete-DDFS-solution could potentially achieve similar or superior performance when employing equivalent or more advanced technologies. The digital structures will benefit from the increase in the cutoff frequency along with CMOS technology scaling as well as a higher integration density and the lower energy per operation [10]. Assuming the ITRS projections, there will be a number of practical problems (if not challenges) when implementing high-speed DM-DDFS architectures in more advanced CMOS technologies.

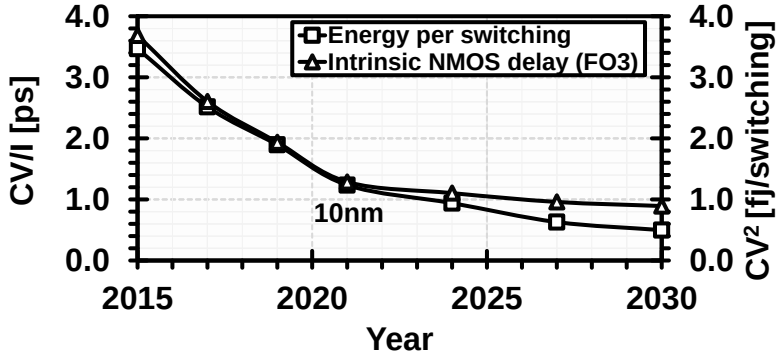


Fig. 7.7. 2015 ITRS logic core device technology roadmap. Intrinsic NMOS delay (CV/I) and energy per switching operation (CV^2).

TABLE 7-3: BENEFITS AND DRAWBACKS OF TECHNOLOGY SCALING

Domain	Digital	Analog
Benefits	The cutoff frequency increases along with CMOS technology scaling [10]	
	Higher integration density	
	Lower energy per operation	
Drawbacks	Power-thermal limitation [82]	SNR degradation due to low voltage operation [10]
	Increasing of the leakage power [82]	Degradation of the mismatch voltage (V_t) [10]
	Decrease of the noise margin [83]	Degradation of *1/f* noise [10]

The increase on the leakage currents, power-thermal density limitations and a reduction of the noise margins could limit the performance of the digital structures [81]-[83]. From the analog performance perspective, degradations in the mismatch voltage (V_t) and the *1/f* noise will impose serious restrictions [10]. Architectures that can achieve a rail-to-rail operation like the proposed 2I-RDAC will be required in order to mitigate the SNR reduction due to a lower voltage operation [10].

Higher levels of interleaving could be used in order to further increase the sampling rate. The throughput of the digital structures can be increased by a factor two when compared to [48], [49] by employing a four-times interleaved RDAC (4I-RDAC) similar to the one represented in Fig. 7.8. As expected, this architecture trade-off performance and area (twice the logic area is required). Also, the number of switches in the RDAC cells need to be increased in order to accommodate the four interleaving channels. A growth in the switching parasitics and a reduction of the sampling window will result in more strict requirements in terms of settling time. Fig. 7.9 represents the simulated full-scale transitions at the differential output of the 2I-RDAC discussed in Chapter 4 when employing different sizes and lengths in the P+ polysilicon resistors and the bonding wire models respectively. It can be observed that, when reducing the resistor area by a factor of two (which represents a drop in the parasitics capacitance of about 4.2fF/unit), an improvement of only 3ps in the slew rate was registered.

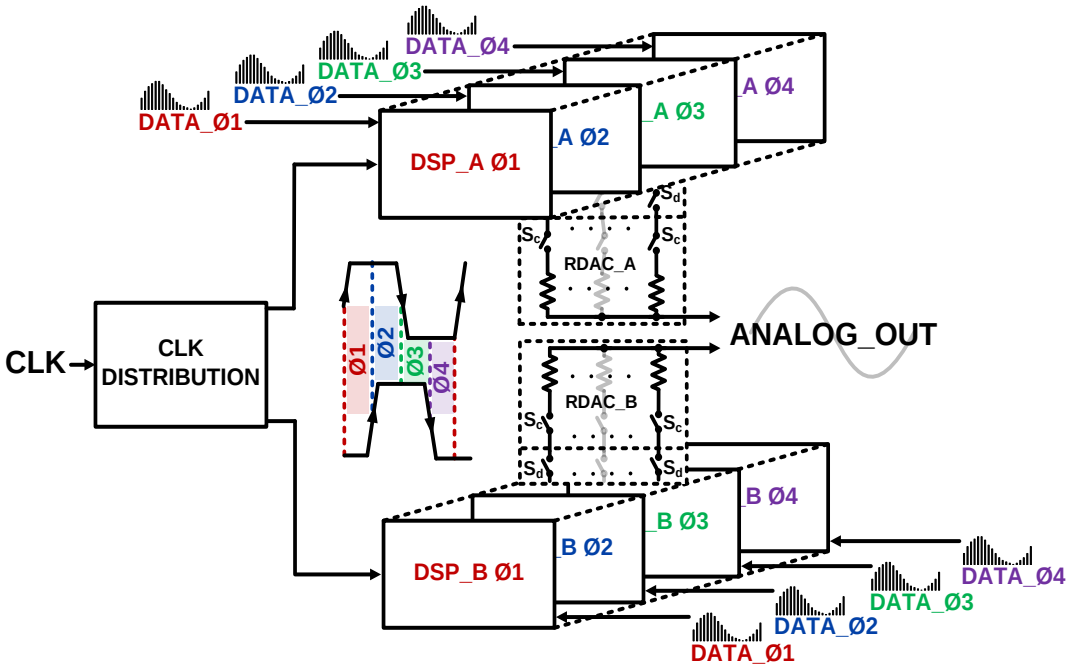


Fig. 7. 8. Four-times interleaved RDAC (4I-RDAC).

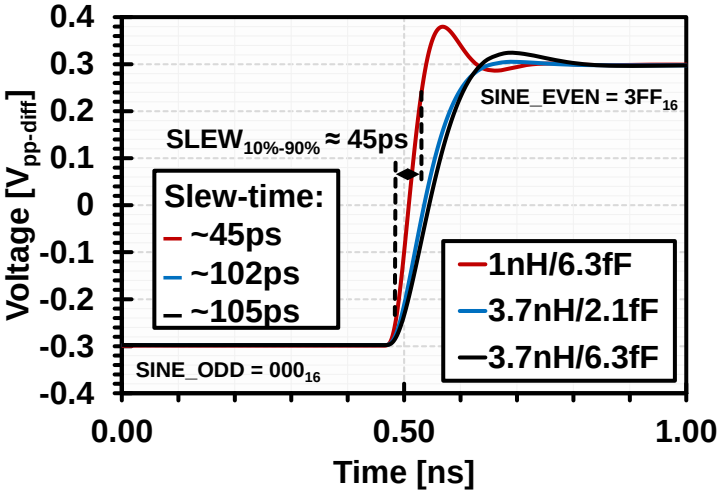


Fig. 7. 9. Simulated settling times. RDAC unit parasitic capacitance ≈ 6.3fF (3.3×12.43μm^2) (3200Ω) and ≈ 2.1fF (1.65×6.215μm^2) (3200Ω). Bonding wire parasitic resistance/inductance ≈ 0.37Ω/3.7nH and ≈ 0.1Ω/1nH (1mm). No power supply noise.

On the other hand, when employing a bonding wire model with 1nH and 0.1Ω (instead of the 3.7nH and 0.37Ω employed in Chapter 4) a reduction of about 57% in the slew rate was observed. This results strongly suggest that a small encapsulate with reduced parasitics will be fundamental in order to support the higher throughput of the four-times interleaved DSP units. The simulated results shows a best case slew-rate of about 45ps which represents 63% of the sampling period at 14GS/s. Another side effect of using a four-times interleaved architecture is that the gain and timing interleaving images are now located at ($F_{CLK}/4 \pm F_{OUT}$) and ($F_{CLK}/2 \pm F_{OUT}$). This fact imposes even more strict requirements on the clock distribution network. Similar to the 2I-RDAC case, the gain mismatch can be reduced by sharing in time a common resistive array among the four interleaved digital phases ($\emptyset_1$- $\emptyset_4$ in Fig. 7.8).

Additional techniques should be also applied in order to lessen the spur contents in the output spectrum. Reduced swing drivers have proved to be a key factor in decreasing the clock feedthrough in data converters [84]. Also, since the interleaving spurs dominate the SFDR performance, duty-cycle calibration techniques should be integrated [74], [85]. In [74] a digitally controlled 2x6-bit capacitor bank can slightly delay two complementary clock signals obtained from a pair of divider circuits (Fig. 7.10). The two SR-latches in Fig. 7.10 convert the time-delayed signals into two anti-phase square waves. A delay-range =±3.3ps with 50fs-55fs steps when running at 1.7GS/s was reported in [74]. Transistor level simulations show a delay-range =±2ps with 43fs steps when running at 7GS/s in the same 65nm CMOS technology employed in this study. This circuit could be employed to compensate the sampling errors caused by the duty cycle distortions introduced by the clock distribution network (3.3ps at

TT/1.2V/25°C according to the transistor level simulation results presented in section 4.3). The energy consumption can be further reduced by employing more sophisticated compression techniques in the PAC block together with the complementary dual-phase sequencing method. One candidate technique is the sine-phase difference algorithm described in [86]. A general block diagram of this implementation is represented in Fig. 7.11. Instead of mapping the first quarter of the *sin(πx/2)* function into logic, the data resulting from (7.1) can be represented in the form of SoP terms. The maximum numerical value of *f(x)* is only 21% of the biggest value in one quarter of the sinusoidal period [85]. For that reason, two fewer bits are needed when mapping the data into SoP terms. However, one extra adder is required in the structure. As demonstrated in this dissertation, significant improvements in terms of throughput and energy efficiency can be achieved by employing the complementary dual-phase latch-based method in a pipelined adder.

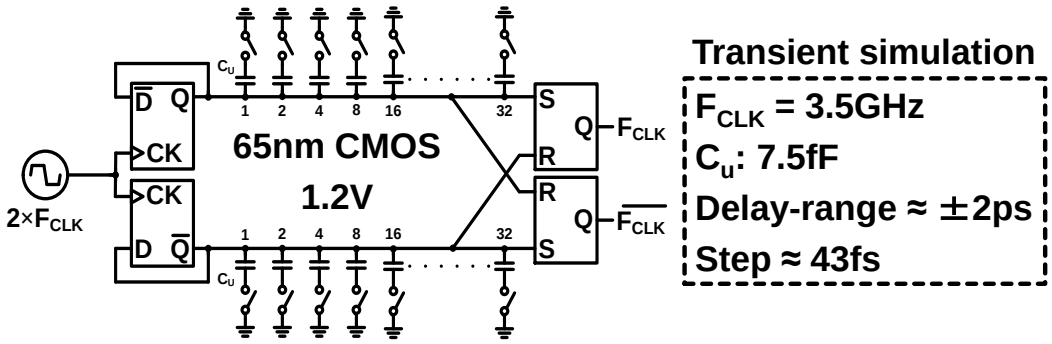


Fig. 7. 10. Duty-cycle calibration technique [74].

$$f(x) = \sin\left(\frac{\pi x}{2}\right) - x \tag{7.1}$$

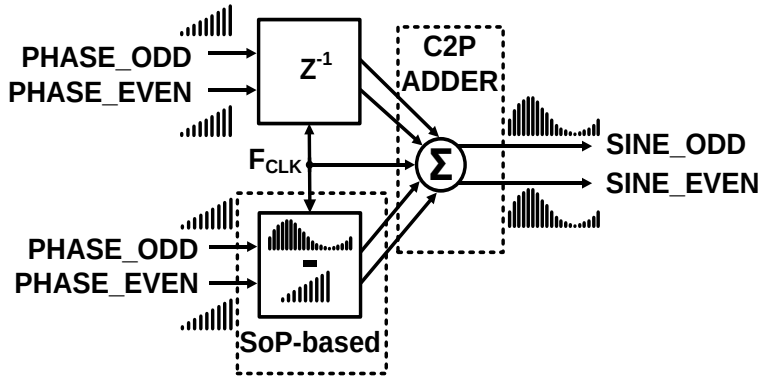


Fig. 7.11. Complementary dual-phase PAC block based on SoP terms and employing the sine-phase difference algorithm.

Consequently, this mechanism could offer savings in terms of area and also power efficiency. The block generating the *f(x)* function can be implemented as a SoP terms based digital circuit. The additional adder can employ the same complementary dual-phase architecture described in Chapter 5 (C2P-ADDER). This architecture is also a feed-forward structure that can be speeded up by employing the time borrowing technique.

Finally, the simple RDAC cells discussed in Chapter 4 constitutes the only analog component in the proposed high-speed DM-DDFS architecture. This structures could be designed by employing standard cells performing analog-like functions. The P-MOS or N-MOS channels composing the logic cells could be employed as N-well resistors resulting in a fully-synthesizable architecture. Consequently, the design times could be reduced by using automatic synthesis, place and route tools. Additional challenges will arise due to the non-linearity introduced by these less precise resistive units. Dynamic element matching techniques could be also employed in order to randomize the non-linear behavior of the synthesizable RDAC cells. The net effect of applying these techniques and at the same time scaling down the CMOS technology could result in future designs falling into the target area represented as region IV if Fig. 7.5. Table 7-4 summarizes the projected trend lines and relates those techniques that could boost a new breakthrough in the DDFS technology based on the result presented in this study.

TABLE 7-4: FUTURE DEVELOPMENT TRENDS AND TECHNIQUES

Features	W-SFDR	Power efficiency	Sampling rate	Design time
Techniques	● Reduced swing drivers ● Duty-cycle calibration	● Sine-phase difference compression mechanism ● Adaptive bias and clock gating	● CMOS technology scaling ● Higher interleaving factors	● Fully synthesizable RDAC cells

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APPENDIX A: PUBLICATION LIST

JOURNAL

- Abdel Martinez Alonso, Masaya Miyahara and Akira Matsuzawa, “A 7GS/s Complete-DDFS-Solution in 65nm CMOS,” *IEICE Transactions on Electronics*, Vol.E101-C, No.4, April 2018. *(Accepted)*

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